AD-A185 856 INSTRUMENT BUS: AN ELECTRONIC SYSTEM ARCHITECTURE FOR OCEANOGRAPHIC INSTRUMENTATION(U) WOODS HOLE OCEANOGRAPHIC INSTITUTION MA E C MELLINGER ET AL. 1/2

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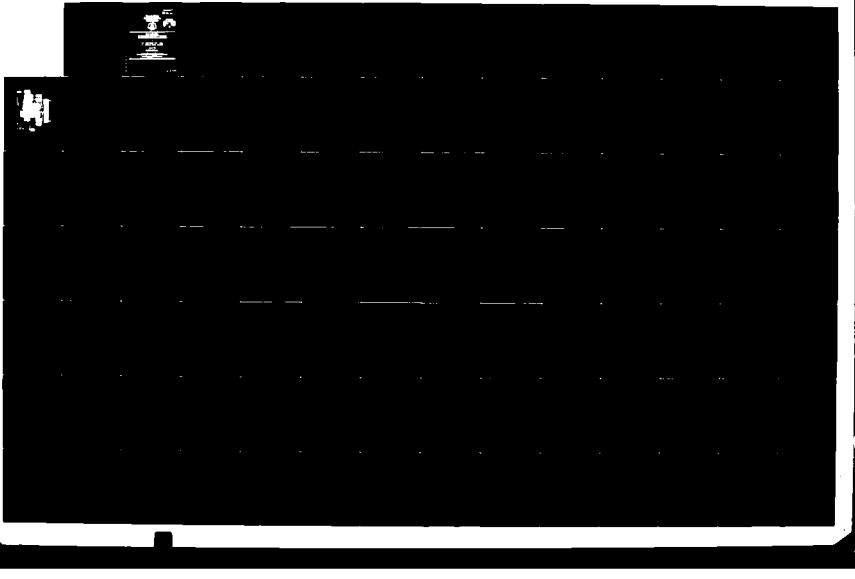

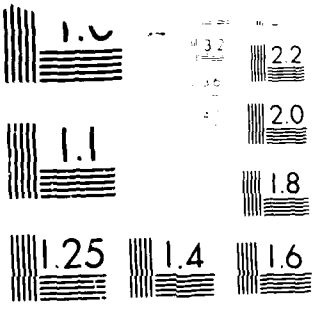
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Instrument Bus
An Electronic System Architecture for Oceanographic Instrumentation

by

E.C. Mellinger, K.E. Prada, R.L. Koehler, K.W. Doherty

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Technical Report

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Approved for Distribution:

Robert C. Spindel, Chairman
Department of Ocean Engineering

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ABSTRACT

A family of electronic and mechanical components has been developed to streamline the process of designing electronic systems for in-situ oceanographic instrumentation. The basis for the family is a card rack designed to fit into 6" I.D. pressure cases, and a companion CMOS computer backplane derived from the IEEE-796 (Multibus) standard. A set of computer boards based on the 80C86 processor was designed and implemented using this architecture. The board set includes the 80C86 CPU, a 64 kbyte memory module, serial and parallel I/O, timebase and counter, and a 16-bit A/D converter. A computer based on this board set consumes 375 mW at 5V while operating with a 5 MHz CPU clock, and 7.5 mW with the CPU clock in STOP mode. In addition to computers, the card rack design can also be adapted to the implementation of other electronic subsystems, including analog front end, mass storage, and power control systems. This report describes the system architecture, gives electronic and mechanical specifications for the backplane and rack, and documents each of the computer boards designed to date. (Summary portions of this report have appeared in the Proceedings of the IEEE Oceans '86 Symposium.)

INTRODUCTION

1.1 Motivation

Electronic design plays a major, and sometimes dominant, role in oceanographic instrument system design. Most of the important sensors employed are of the sensed-parameter-to-electrical-parameter variety, and require careful signal conditioning to capture useful information from the raw sensor output. Most conditioned sensor data is digitized in-situ, for further analysis, for storage, or for telemetry. Digitized data is manipulated by the ubiquitous microprocessor, which also performs numerous control and supervisory functions in the instrument system. Even instruments which are largely mechanical employ electronic subsystems for power conversion, actuator drive, and general control. The need to efficiently apply electronic techniques is a key requirement of modern instrument system design.

Design work in the Department of Ocean Engineering (OE) at Woods Hole Oceanographic Institution includes the creation of several new instrument systems each year. The search for flexibility and economy in the design of instrumentation electronics led a group of engineers in the OE Department to explore the concept of mechanical and electronic modularity in instrument design. It was observed that a tendency had developed to invent a new electronic architecture for each new instrument, typically including a new controller/processor, set of support electronics, and packaging scheme. This required a fair amount of engineering time, and increased the development cost of each new system. Although modularity was a far-from-novel concept, a reassertion of its value in instrument system design seemed timely.

The justification for new electronic designs nearly always involved insufficient flexibility in existing designs. This in turn stemmed from a lack of modularity in the existing designs, and a lack of generality in the definition of those modules that did exist. Underlying these symptoms was the lack of a unifying concept, or architecture, that could encompass a broad range of instrument applications; specifically a mechanical and electronic framework that could form the basis for a set of "building block" modular components. Our group thus undertook the definition of a foundation upon which such instrument system components could be built. Our goal was to provide the architectural basis for a "kit of parts" which could be used off-the-shelf to implement substantial portions of new instrument systems. This would free designer attention for the application specific portion of each project, and ensure that new application specific building blocks could be used by other projects in the future.

The outstanding question was what mechanical and electronic attributes of the instrument system to standardize. Electronic systems, and their modular components, divide easily (though usually not neatly) into predominantly-analog and predominantly-digital subsystems. Examples of the former include front-end signal conditioning circuits (preamps, filters, receivers, digitizers) and power control and conditioning circuits (actuator drivers, power amplifiers, transmitters, power supplies). Examples of the latter include processor-based subsystems (controllers, signal processors) and mass storage units (solid state, magnetic, optical). For analog function modules, standardization is effectively limited to the definition of packaging and interconnection formats by the point-to-point, signal-specific nature of

analog circuits. Processor-oriented digital function modules can standardize at a more detailed level, as in the definition of computer backplanes to which processors, memories, and I/O devices can all connect. As an initial effort, our group decided to focus on two areas: first, a packaging and interconnection scheme of sufficient generality to address all of the analog and digital applications mentioned above; and second, a digital processor backplane around which a family of computer components could be built.

This report describes in detail the specifications for the rack package and backplane which are the initial implementation of the Instrument Bus architecture. Two points should be made before delving into the technical issues. The first is that the computer backplane was defined first partly due to a pressing need, and partly because it was the easiest item of electronic architecture to standardize. However, it may also be possible to define a kind of analog backplane, where signal conditioning boards could supply signals to a digitizer; or a power control backplane, optimized for noise immunity and high current and voltage capability; or a video processing backplane; or other kinds of application-specific interconnect standards, all based on the packaging format defined here. We encourage anyone who is interested to apply and extend the concepts presented here.

The second point is that the Instrument Bus was conceived to make life easier for oceanographic instrument designers. It is not a rigid and extensive set of rules with which one must comply, not a grand philosophy which one must embrace, not a series of tests which one must pass to receive some special annointment. It is not a way of selling computer boards. It is, really, just an approach to designing instrumentation; a center of gravity around which we hope that a body of technique will accumulate. Extensions, adaptations, modifications, and even corruptions of the standards proposed here will be welcome, as long as they facilitate the creation of instrument systems, and leave a legacy which is of benefit to other members of the design community.

1.2 Design Requirements

Packaging considerations provided the primary constraint for the development of the Instrument Bus concept. It was assumed from the outset that full ocean depth (6000 meter) capability would be required by a significant fraction of instrument system designs in the future. Considerable debate therefore went into the issue of pressure case size. In the end, the ease of handling (ashore and at sea) of the 6" ID cylindrical configuration won out over the electronic packaging efficiency offered by larger tube sizes, particularly 10" ID. The volume penalty imposed by the smaller tube size was felt to be offset by the the observed tendency of integrated circuit and mass storage device density to double every few years, plus the expected advent of high density surface mount packaging for electronic devices.

The electronic performance goals for instrument systems to be implemented using the Instrument Bus approach spanned a broad range. At the low end, in terms of complexity and computer processing power, are battery-powered instruments and systems intended for multiyear deployments. These typically make a few measurements per hour, perform minimal in-situ processing, and record or telemeter modest quantities of data. The design emphases are usually reliability, low energy consumption, and low cost. At the other end

of the performance spectrum are complex, computation and/or energy intensive applications such as doppler current meters, acoustic imaging systems, vehicle control and guidance systems, and feature extraction or pattern recognition systems. These systems either have large data bandwidths, control large amounts of power, and/or must operate in real time. The design emphasis is on maximizing electronic performance, with cost and energy efficiency assuming secondary importance. Since the low end applications are reasonably well served by existing data-logger approaches, most of our effort went into developing the flexibility to handle the high end applications, without unduly compromising the cost or energy performance of low end implementations.

Consideration of the packaging and performance goals outlined above led to the following set of requirements and/or desireable features for the Instrument Bus architecture:

1. With respect to a cylindrical pressure case, plug-in circuit cards would be oriented crosswise, perpendicular to the tube axis, and the backplane or connector plane would be oriented lengthwise, parallel to the tube axis. A card rack and card form factor standard, similar to the familiar 6" D-Card, would define connector placement, cable routing, and card support, and ensure mechanical interchangeability of the circuit cards. Use of a two-piece, as opposed to card-edge, connector would maximize interconnect density and contact reliability.

2. The processor backplane architecture would be computer bus based, in the conventional sense of a backplane supporting communication between plug-in processor, memory, and I/O modules. Definition of a completely new bus standard was considered unwise.

3. The backplane specification would be general enough to allow use of processors from several different manufacturers. A non-multiplexed 16-bit data path was required for computation-intensive applications; the ability to also work with 8-bit processors and peripherals would be an asset. Memory space in the megabyte range was required for large programs and data sets. Multiprocessor capability would also be an asset.

4. The bus signal electrical specifications would be based on static CMOS interface and logic devices, as would all board designs intended for long-term deployment applications. (The fixed-energy-per-clock-cycle characteristic of CMOS ties power consumtion to performance level and places them under the designer's control. Low power operation, at reduced throughput, is possible even for a high performance 16-bit backplane architecture.)

1.3 Backplane Selection

A review of existing computer-bus specifications revealed no candidate that could be adopted without modification. The primary contenders were the existing CMOS backplanes, particularly C-44 [1], CIMBUS [2], and CMOS STD [3], which offered some hope of an off-the-shelf solution. These 8-bit bus standards serve well for the implementation of controllers and data loggers, but their limited bandwidth makes them less suitable for computation-intensive or real time applications. More importantly, their packaging form factor requires the cards to lie lengthwise and the backplane to lie crosswise when installed in a 6" ID tube, leading to an awkward situation when the bus must

be extended to more than four or five cards. A C-44 modification to D-card format was seriously considered, but this negated the existing board set which was C-44's primary advantage, while retaining the multiplexed 8-bit architecture which was its primary disadvantage.

In early 1984, existing 16-bit backplanes were limited to IEEE-796 (Multibus) [4] and VME [5]. Both have large card form factors and TTL-based bus specifications, so extensive adaptation would be required to meet the packaging and energy constraints outlined above. However, both also have high-bandwidth, large-memory-space, multiprocessor architectures capable of meeting the target performance requirements for Instrument Bus processor systems. In the end, IEEE-796 was selected on the basis of greater flexiblity in the instrumentation environment; specifically this included the ability to work with either 8 or 16 bit devices (or both), and the ability to support a wide variety of processor families.

Adapting the IEEE-796 specification to oceanographic instrumentation, along the guidelines outlined above, involved the following steps:

Selection of a rack and backplane configuration

This included the rack itself, the backplane connector, and the circuit board form factor. As mentioned, the overall packaging approach was intended to be useful in the implementation of a variety of electronic subsystems in addition to the computer; the detailed design considerations are described in section 3 below. The backplane connector was the subject of an intensive search involving more than 100 manufacturers, with the goal of locating a connector with the following general characteristics:

A) a density of 75 to 100 contacts in a length of 3" to 4";
B) a shock and vibration tolerance in the 10*g* to 20*g* range, suitable for shipboard and over-the-side handling mishaps;
C) a humidity rating to 100% RH, and suitable for brief exposure to salt atmosphere;
D) a contact life of several hundred mating cycles;
E) a reasonable cost, of order $0.10 per mated line.

The search turned up a suprising number of high quality connectors, nearly all of them single-sourced by small manufacturers. The DIN 41612 Style C connector, popularly known as the "Euroconnector", emerged as the only widely available component. The 3.7" length of this 96-pin connector fits well in the 6" ID pressure case, and its industrial origins have endowed it with a good level of ruggedness and reliability at a modest price. (As a bonus, other connector styles in the DIN 41612 series, e.g. D and M, have the same mounting dimensions but offer alternate contact configurations, including high current and coaxial contacts.) The dimensions of the DIN connector were used to finalize the specifications for the card rack, and to establish the shape and dimensions of a new 6" D-card for use in this rack. A printed circuit backplane using the Style C connector was developed for the computer application; the backplane allows board connectors to be placed in 0.3" spacing increments , e.g. 0.6", 0.9", 1.2".

Adaptation of IEEE-796 for CMOS bus levels

The changes made from the full IEEE standard are described in section 3 of this report, and summarized here. Standard HC-CMOS input thresholds (0.45 x Vdd) are used to maximize noise immunity on the bus. Since CMOS does not have the DC fanout/fanin constraints of TTL, redefining the bus driver specification was largely a matter of setting maximum allowable bus signal capacitance, and specifying bus drivers capable of driving this load. Characteristic impedance bus termination is not required by IEEE-796, but would have been ruled out in any event by the low power requirement. With a maximum bus electrical length of 3 nsec and typical HC-series CMOS rise/fall times of 5 nsec, reflections are not a major worry. Open-collector (or open-drain) pullup values may be changed by the system designer to accomodate a variety of speed-power requirements.

MECHANICAL SPECIFICATION

2.1 Design Description

The rack-oriented packaging approach indicated in the Requirements section above breaks little new ground in design philosophy, since the general concept has been in use for years and is familiar to most practicioners. It nevertheless proved possible to make a number of significant refinements to existing rack-based approaches. The principal motivation for a new rack design was the DIN 41612 connector family selected as the standard backplane connector for Instrument Bus systems. The new connector dictated a specific circuit board shape, support rail spacing, and general configuration of the rack, and hence, a new rack design. The principal goal for the new design was decreased fabrication cost, in comparision with existing designs which were precision machined from solid aluminum plate and flat bar. A design was sought which required only simple machining operations during assembly; this has the addtional benefit of reducing the lead time required for rack construction. Secondary goals were to decrease the side rail (card guide) deflection in long racks, to use insulating card guides, to add a cable race to protect interconnect cables, and to avoid increasing the overall rack weight or decreasing the active area of circuit boards in the rack.

The design was implemented using bent aluminum plate and extruded aluminum bar. The aluminum plates are formed with all holes and cut-outs prepunched and with threaded inserts installed. The plates can be fabricated in quantity by commercial sheet metal shops; no additional machining is required at rack assembly time. The card guide and backplane rails are extruded aluminum sections. To increase stiffness, the rails conform to the curvature of the pressure case inside wall; this allows material to be placed where needed to increase the moment of inertia without increasing weight or decreasing circuit board size. Figures 1 and 2 show the complete rack assembly with computer boards installed; Figure 3 shows a single computer board.

Figure 1
Card Rack, Front View

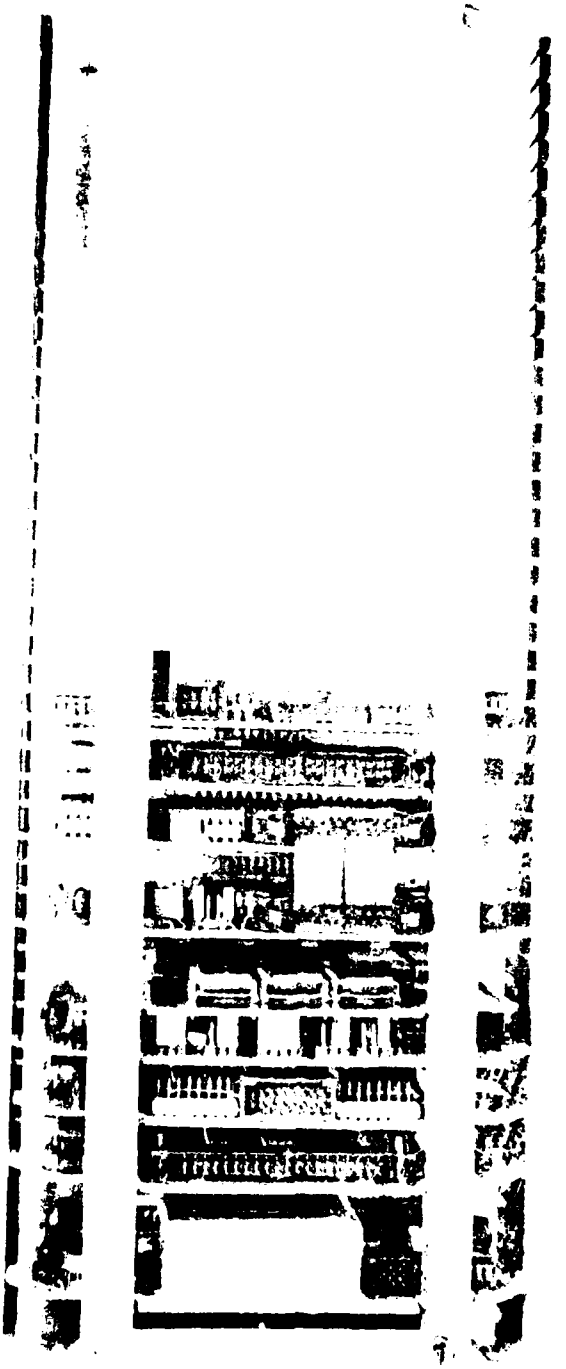


Figure 2
Card Rack, Rear View

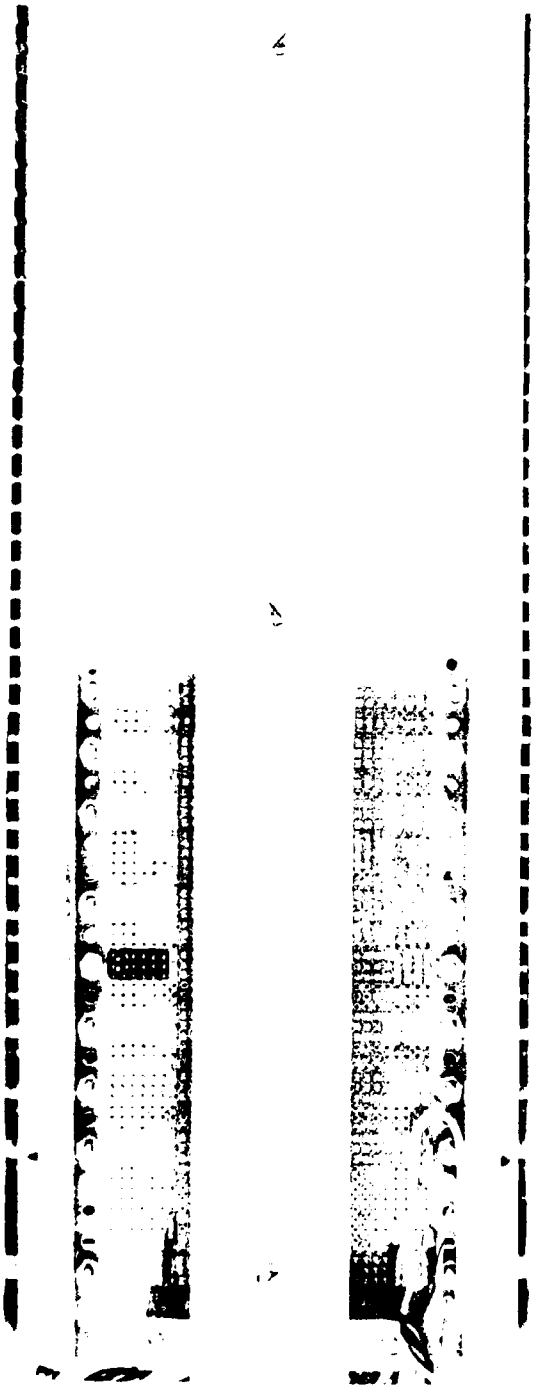
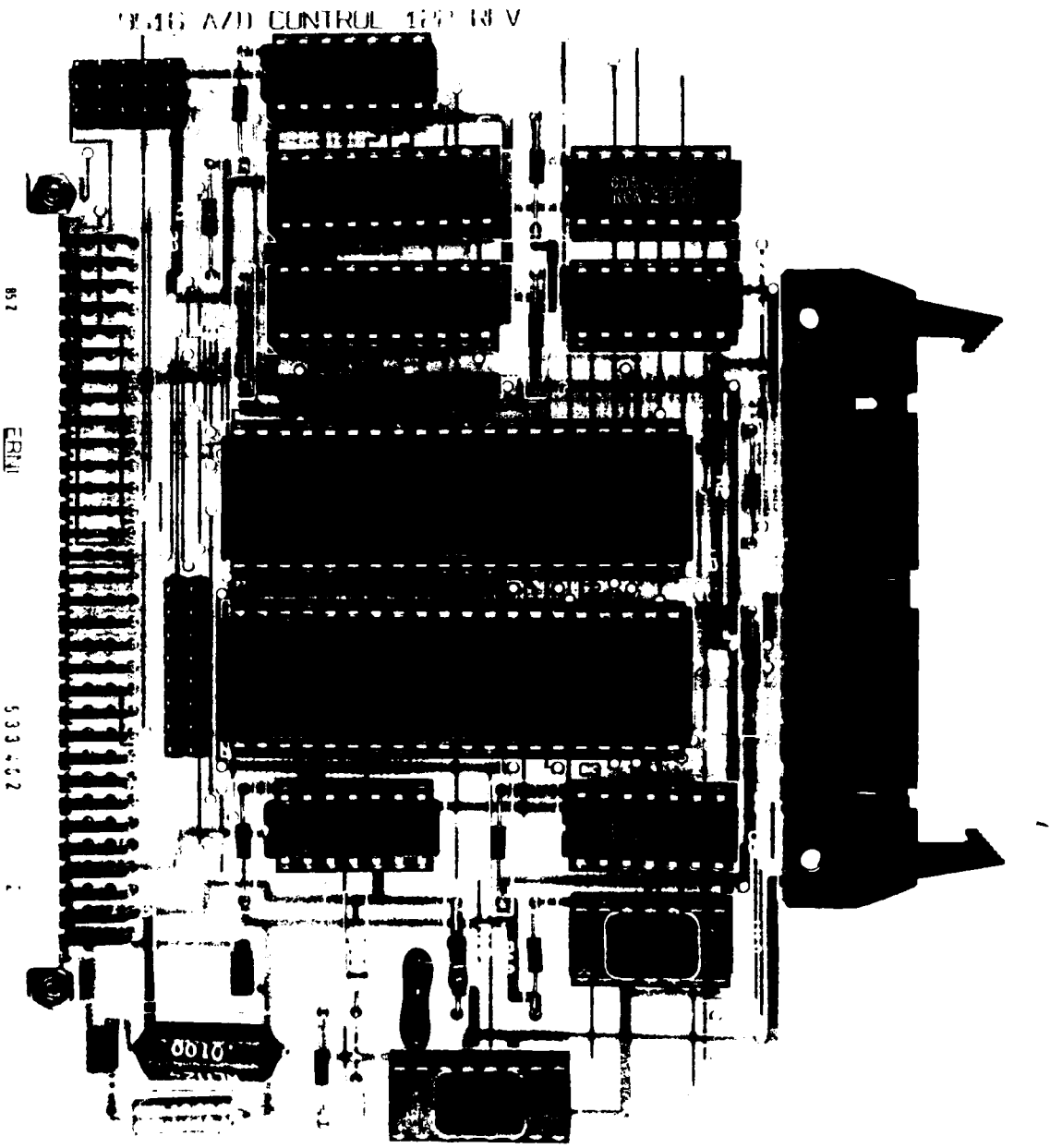


Figure 3
Typical Circuit Board



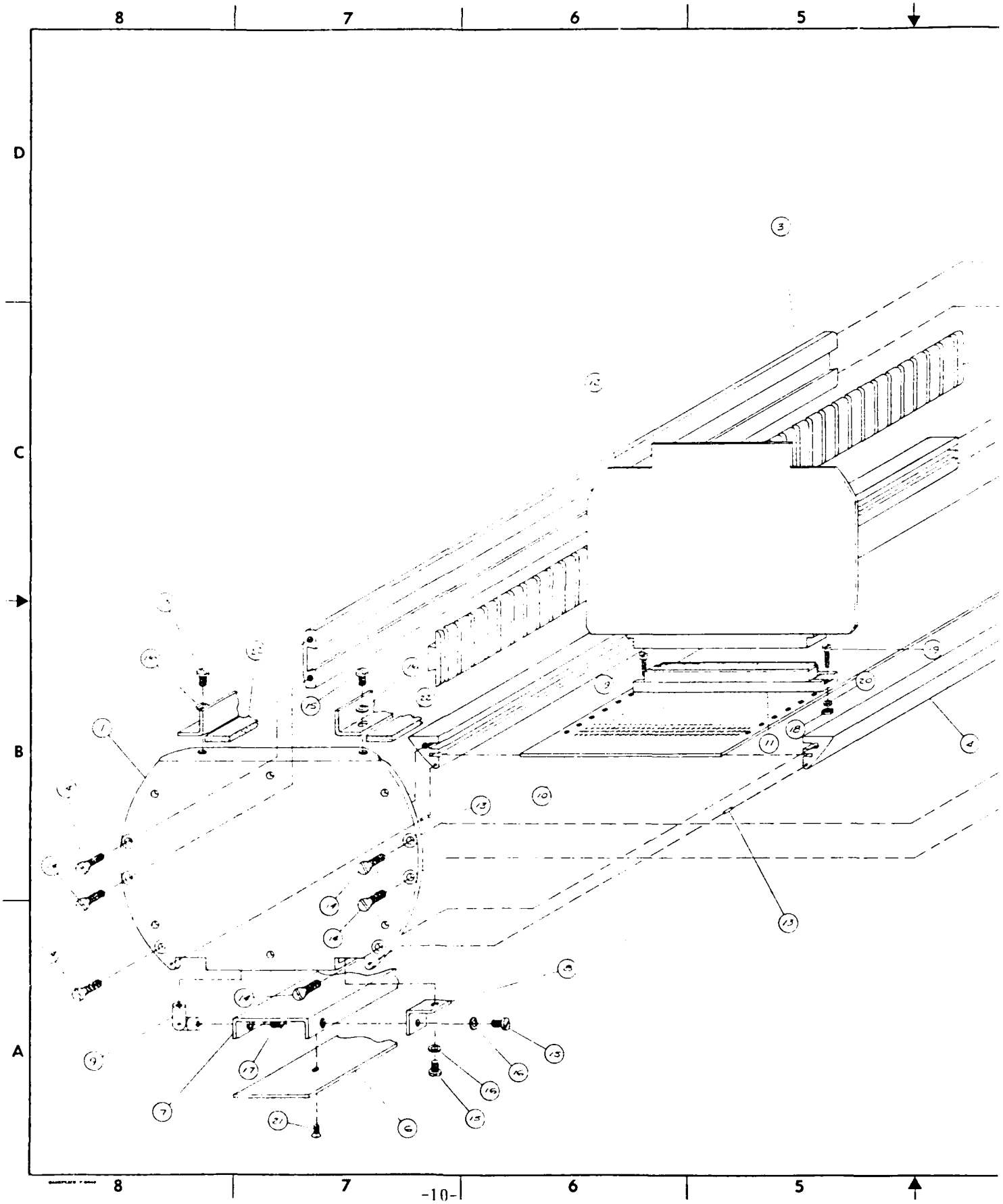
To assemble a single modular rack, two end plates, two side rails with plastic card guide inserts, two backplane rails, and two card retainer angle bars are needed, along with a suitable backplane circuit board. The rails must be accurately cut to length and then drilled and tapped on the ends. The rack can then be assembled with a screwdriver. If a cable race is needed, two additional prefabricated parts are required. It should be noted that two or more modular rack units may be joined (e.g., to marry an analog front end with a computer) simply by bolting the two adjacent endplates back to back through existing prepunched holes.

2.2 Rack Drawings

This section contains detailed mechanical drawings for the components of the Instrument Bus card rack. For reference, Table 1 lists the drawing names and numbers. Assembly drawing D-256 shows the arrangement of the individual components, and provides a parts list for the entire rack assembly.

TABLE 1
INSTRUMENT BUS MECHANICAL DRAWINGS

name	drawing number
Card Rack, Assembly and Parts List	D-256
End Plate	C-409
Card Guide	C-441
Rail, Card Guide, Extrusion	B-942
Rail, Card Guide, Machine Drawing	B-941
Rail, Backplane, Extrusion	B-786
Rail, Backplane, Machine Drawing	B-940
Card Retainer	B-805
Cover, Cable Race	B-804
Cable Race Blank	C-408
Bracket	B-803
Backplane and Chassis Relationship	B-884
Circuit Board Dimensions and Legend	C-465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REVISIONS				
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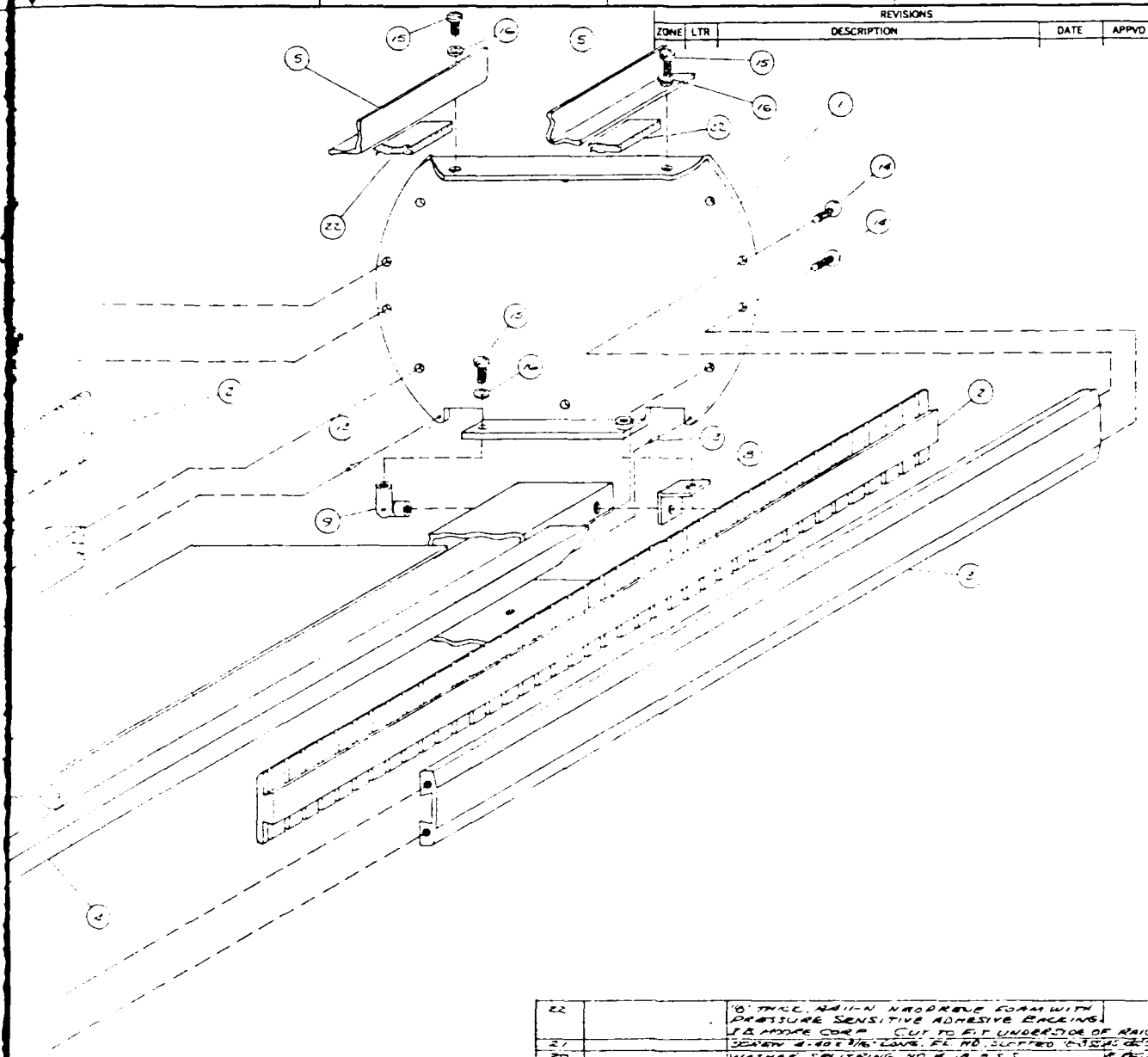

ITEM	PART OR DWG. NO	DESCRIPTION	QTY
22		1/8" THICK NEOPRENE FOAM WITH PRESSURE SENSITIVE ADHESIVE BACKING & HONEYCOMB CUT TO FIT UNDERSIDE OF RAIL	
21		SCREW 4-40 x 3/16" LONG, FL HD, SLOTTED, S.S.	AS REQ'D
20		WASHER, SPLITRING, NO. 4, 18-8 S.S.	AS REQ'D
19		SCREW, 4-40 x 3/8" LONG, FL HD, SLOTTED, S.S.	AS REQ'D
18		NUT, CRS HEX, 4-40 18-8 S.S.	AS REQ'D
17		SCREW, 6-32 x 3/16" LONG, FL HD, SLOTTED, NAS	2
16		WASHER, SPLITRING, NO. 6, 18-8 S.S.	10
15		SCREW 6-32 x 1/4" LONG PAN HD SLOTTED NAS	10
14		SCREW 6-32 x 3/8" LONG, FL HD, SLOTTED 18-8 S.S.	16
13		PIN ROLL, 1/16 O.D. x 1/8" LONG (MAY BE SAWN)	4
12	C-00965	CIRCUIT BOARD	AS REQ'D
11		CONNECTOR, DIN 41612	AS REQ'D
10	B-00944	CAGE PLANE	1
9		MOUNTED STANCOR KEYSTONE NO. 553	2
8	B-00965	BRACKET	2
7	C-00909	CABLE RACK	1
6	B-00943	COVER	1
5	B-00945	CARD RETAINER	2
4	B-00940	RAIL, RACK PLANE	2
3	B-00944	RAIL, CARD GUIDE	2
2	C-00941	CARD GUIDE	8
1	C-00940	END PLATE	4 PAIRS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		CONTRACT NO	WOODS HOLE OCEANOGRAPHIC INSTITUTION OCEAN ENGINEERING DEPT. WOODS HOLE, MA. 02543	
TOLERANCES FRAC DECIMALS ANGLES XX ± ° XXX ±	SURFACE MICRO IN ✓	APPROVALS DATE DRAWN R.D.F. 4/12/84 CHK'D APPV'D	TITLE ELECTRONIC CARD RACK ASSY. & PARTS LIST	
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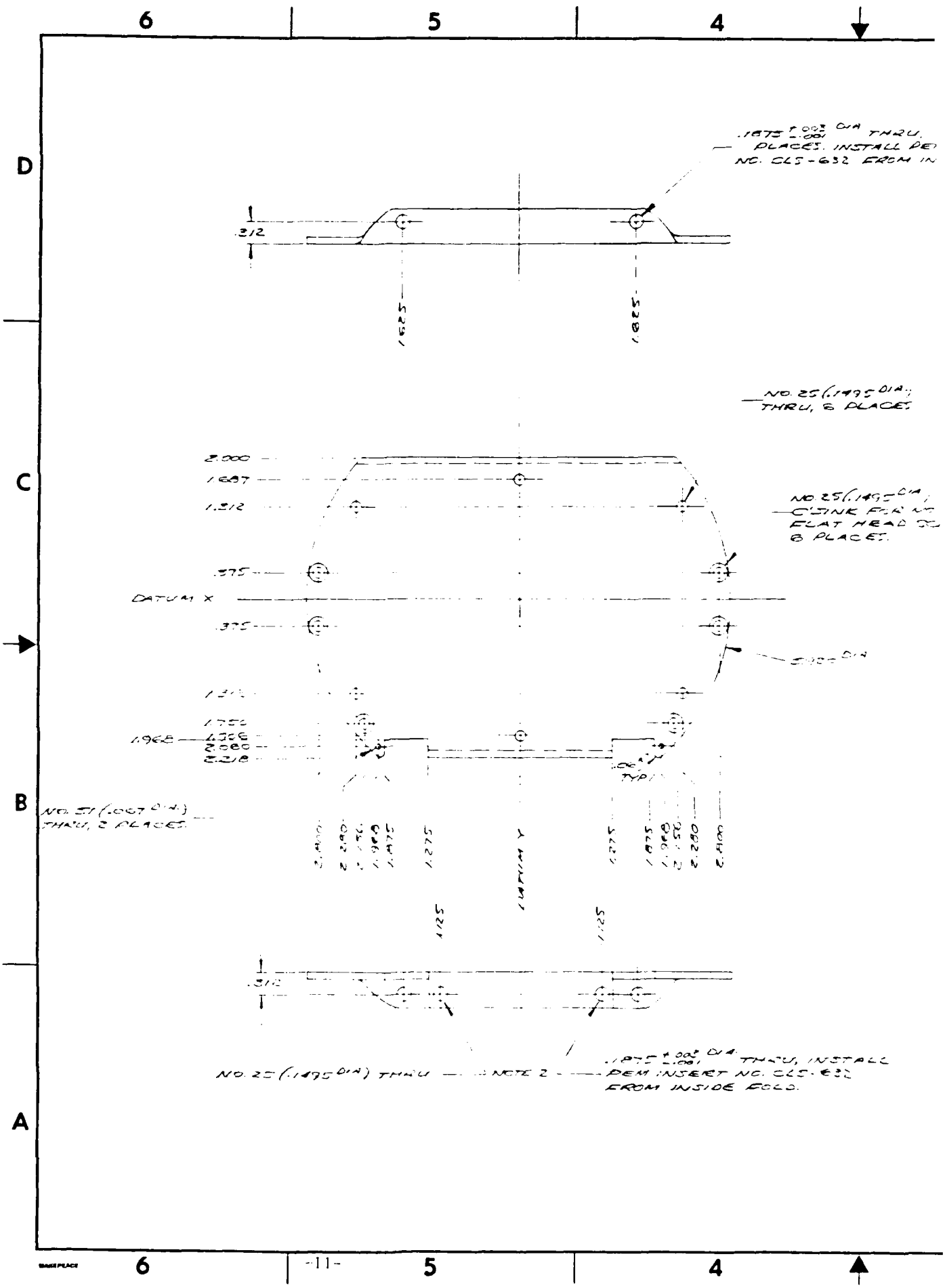
6
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.1875 +.002 -.001 DIA THRU, 2 PLACES. INSTALL REM INSERT NO. CLS-632 FROM INSIDE EQUIP.
.312
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NO. 25 (.1495 DIA) THRU, 6 PLACES
NO. 25 (.1495 DIA) THRU, C'SINK FOR NO. 6 FLAT HEAD SCREW, 6 PLACES.
2.000
1.687
1.312
.375
DATUM X
.375
.5625 DIA
1.312
1.750
1.968
.937
2.060
2.218
90° TYP.
NO. 51 (.067 DIA) THRU, 2 PLACES.
2.400
2.290
1.968
1.875
1.275
DATUM Y
1.275
1.875
1.968
2.280
2.400
1.125
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.312
NO. 25 (.1495 DIA) THRU
NOTE 2
.1875 +.002 -.001 DIA THRU, INSTALL REM INSERT NO. CLS-632 FROM INSIDE EQUIP.

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1. CAUSTIC ETCH & GOLD IRIDITE FINISH.
2. END PLATES ARE DESIGNED IN PAIRS (LEFT HAND PLATE SHOWN). REVERSE THESE TWO HOLES IN RIGHT HAND PLATE.

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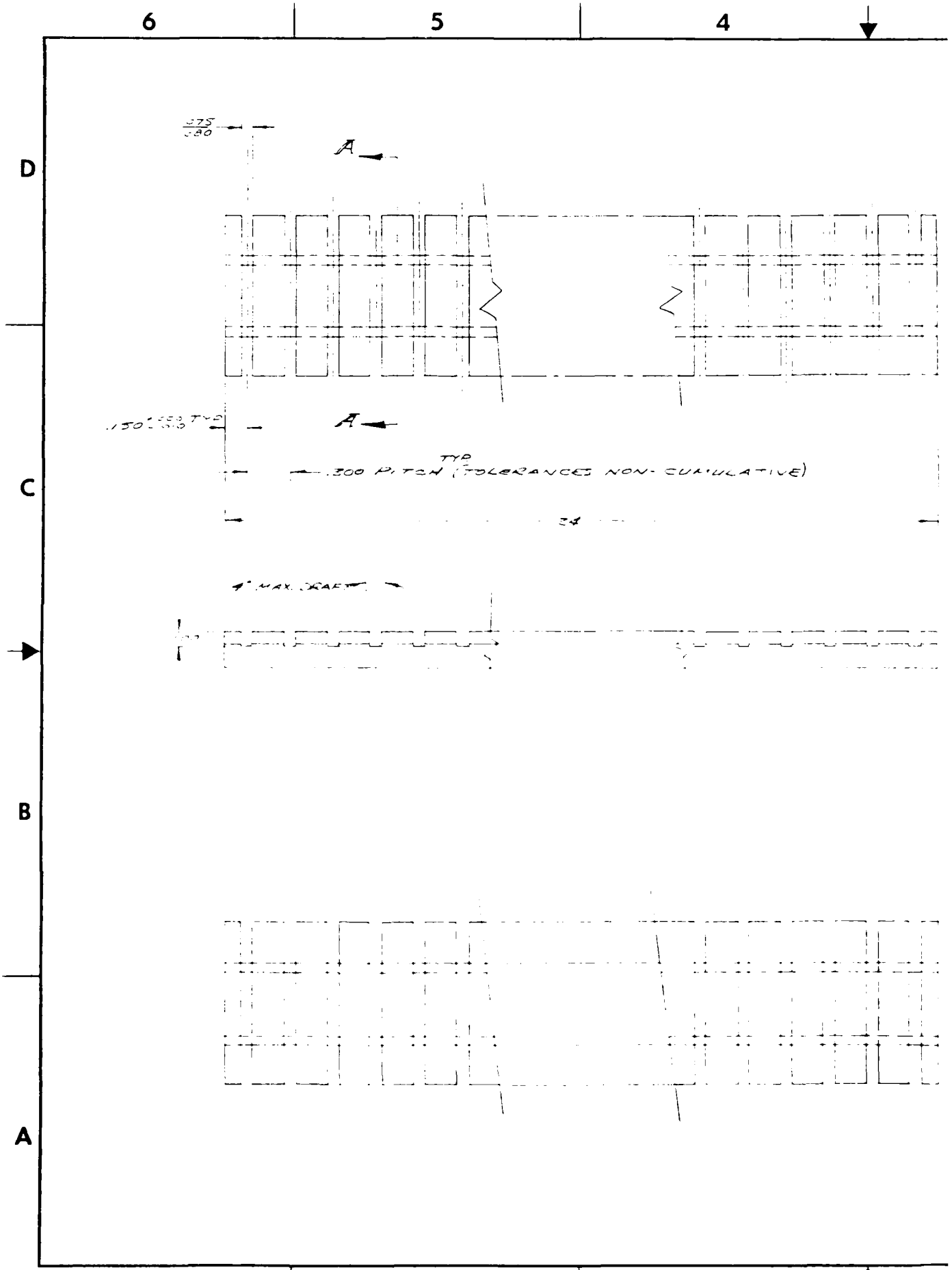
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO 15152.06	WOODS HOLE OCEANOGRAPHIC INSTITUTION OCEAN ENGINEERING DEPT. WOODS HOLE, MA. 02543	
TOLERANCES: FRAC DECIMALS ANGLES SURFACE MICRO IN ✓	APPROVALS / DATE DRAWN KOF 8/22/86 CHK'D APPVD	TITLE: END PLATE	
MATERIAL: 3/32" THICK 5052-H32 ALUMINUM	FINISH: SEE NOTE 1	SIZE C · DWG NO 0469 · REV A	
		SCALE FULL · SHEET OF	


6
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.275
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.150 TYP
.300 PITCH TYP (TOLERANCES NON-CUMULATIVE)
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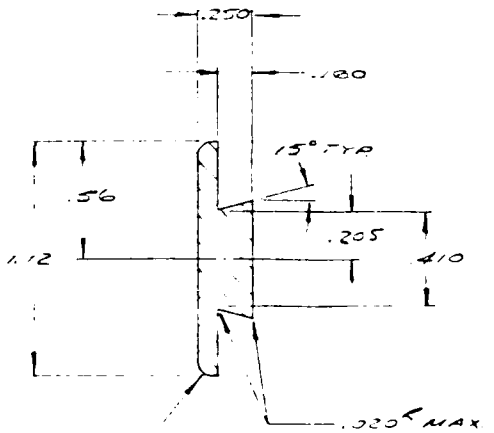
ZONE	LTR	DESCRIPTION	DATE	APPVD



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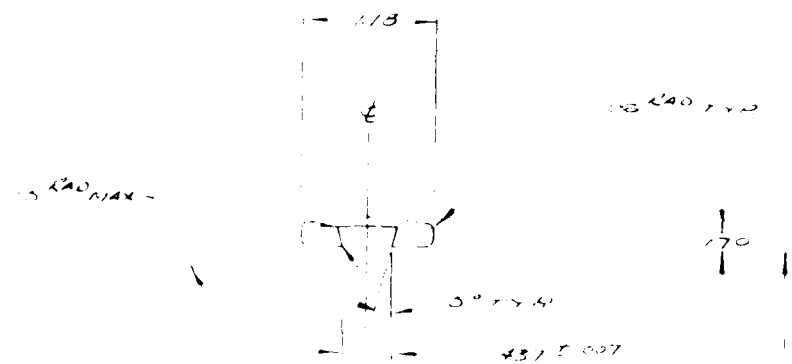
SECTION A-A

ITEM	PART OR DWG. NO.	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRAC DECIMALS XX ± .015 ANGLES ± 1/2° XXX ± .005 SURFACE MICRO IN ✓ MATERIAL 1/4" THICK 141 BLACK LEXAN	CONTRACT NO. 10/82.06 APPROVALS DATE DRAWN KOF CHK'D APPVD FINISH	WOODS HOLE OCEANOGRAPHIC INSTITUTION OCEAN ENGINEERING DEPT. WOODS HOLE, MA. 02543 TITLE CARD GUIDE SIZE C DWG. NO. 00441 REV SCALE 1:2 SHEET OF	

DWG NO

MS



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD

ITEM	PART OR DWG. NO.	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES: FRAC DECIMALS ANGLES ± 1°

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MATERIAL 6063-T52 ALUMINUM ALLOY

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DRAWN EDF	9/27/96
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FINISH NONE

WOODS HOLE OCEANOGRAPHIC INSTITUTION
OCEAN ENGINEERING DEPT.
WOODS HOLE, MA. 02543

TITLE RAIL CARD SLIDE EXTRUSION

SIZE B | DWG. NO. 00942 | REV.

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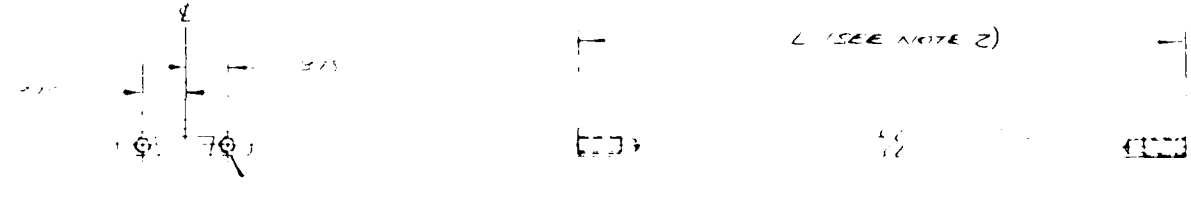

-14-

NOTES
1. [illegible]
2. LENGTH L [illegible]

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD

ITEM	PART OR DWG NO	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: FRAC DECIMALS XX ± ANGLES ° XXX ±
SURFACE MICRO IN ✓
MATERIAL EXTRUSION ONLY NO B-CODE
CONTRACT NO. 10/86.02
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FINISH SEE NOTE 1

WOODS HOLE OCEANOGRAPHIC INSTITUTION
OCEAN ENGINEERING DEPT.
WOODS HOLE, MA. 02543

TITLE RAIL, CABLE GUIDE MACHINE DWG.

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ZONE	LTR	DESCRIPTION	DATE	APPVD

ITEM	PART OR DWG NO	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES:
FRAC DECIMALS
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FINISH	

WOODS HOLE OCEANOGRAPHIC INSTITUTION
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WOODS HOLE, MA. 02543

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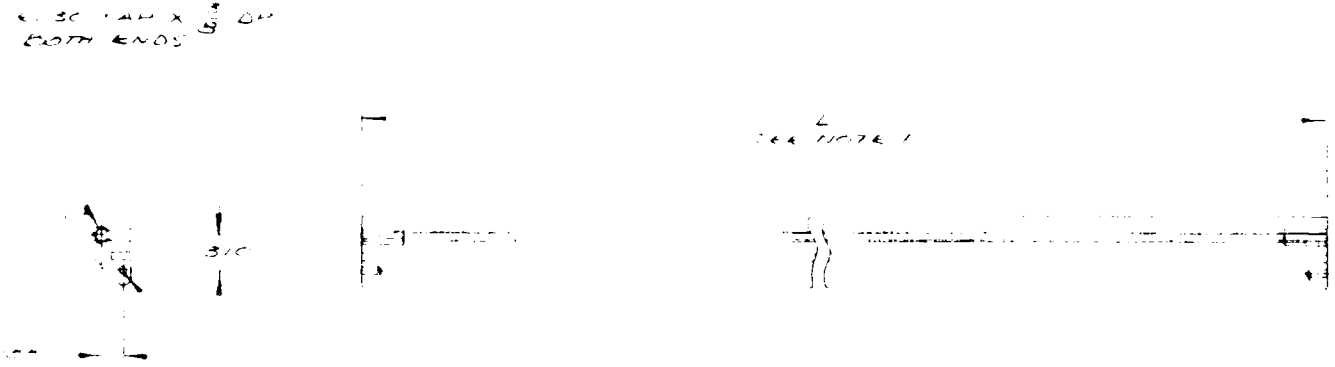
SCALE 3:1 | SHEET OF

MARESPACE P 8078

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD



ITEM	PART OR DWG NO	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRAC DECIMALS .XX ± ANGLES ° .XXX ± SURFACE MICRO IN ✓ MATERIAL	CONTRACT NO APPROVALS / DATE DRAWN / CHK'D / APPVD FINISH	WOODS HOLE OCEANOGRAPHIC INSTITUTION OCEAN ENGINEERING DEPT. WOODS HOLE, MA. 02543 TITLE SIZE / DWG NO / REV SCALE / SHEET / OF

MADEPEACE P 6075

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD

ITEM	PART OR DWG NO	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES: FRAC DECIMALS ANGLES XX ± .1 XXX ± .05

SURFACE MICRO IN ✓

MATERIAL 5052-H32 ALUMINUM

CONTRACT NO

APPROVALS	DATE
DRAWN	
CHK'D	
APPVD	

FINISH SEE NOTE 1

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TITLE

SIZE B | DWG. NO. 00805 | REV.

SCALE FULL | SHEET OF

MADEPEACE P.8078

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD

ITEM	PART OR DWG NO	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES

FRAC DECIMALS

XX ±

ANGLES ° XXX ±

SURFACE MICRO IN

MATERIAL

CONTRACT NO

APPROVALS DATE

DRAWN

CHK'D

APPVD

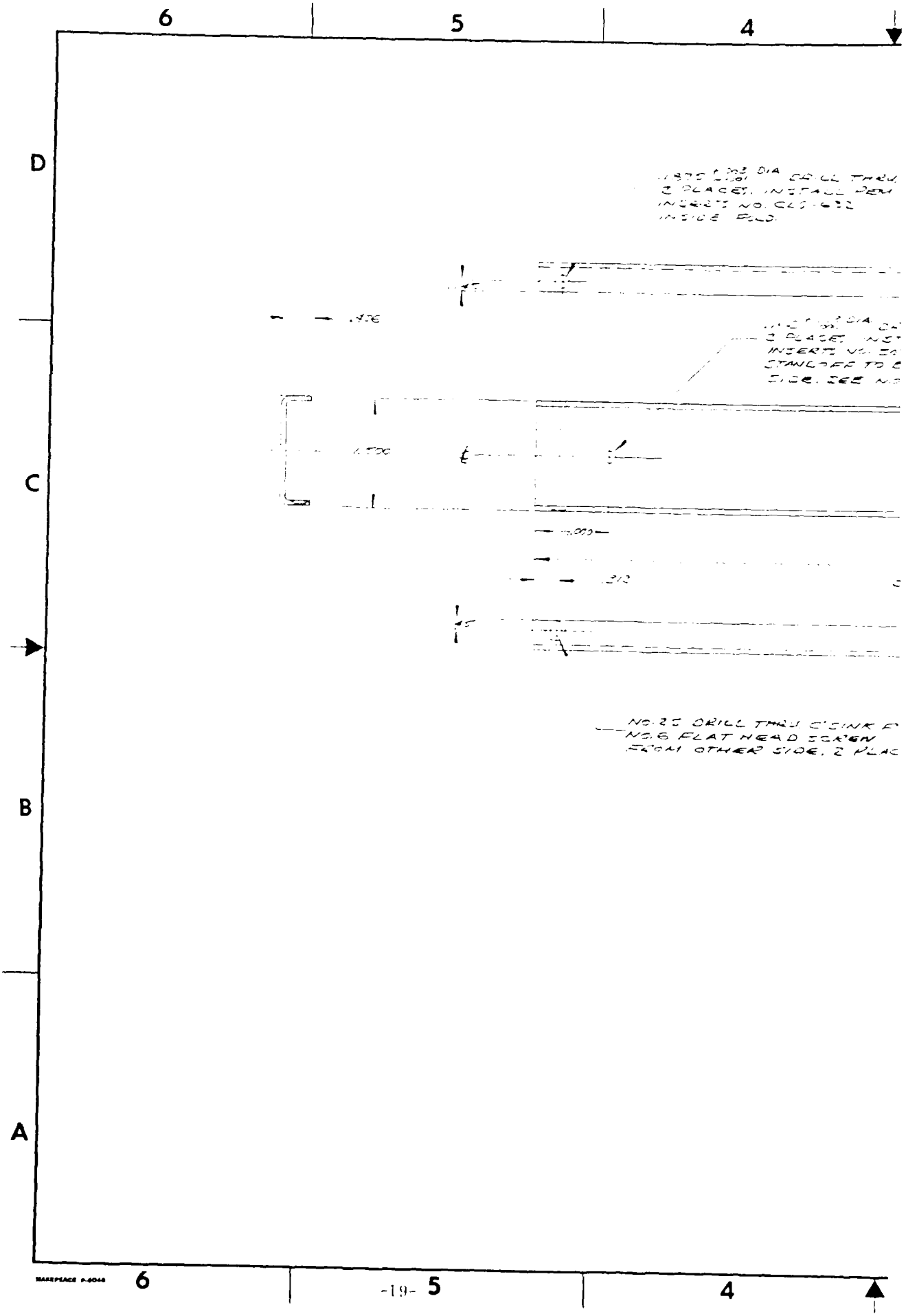
FINISH

WOODS HOLE OCEANOGRAPHIC INSTITUTION
OCEAN ENGINEERING DEPT.
WOODS HOLE, MA. 02543

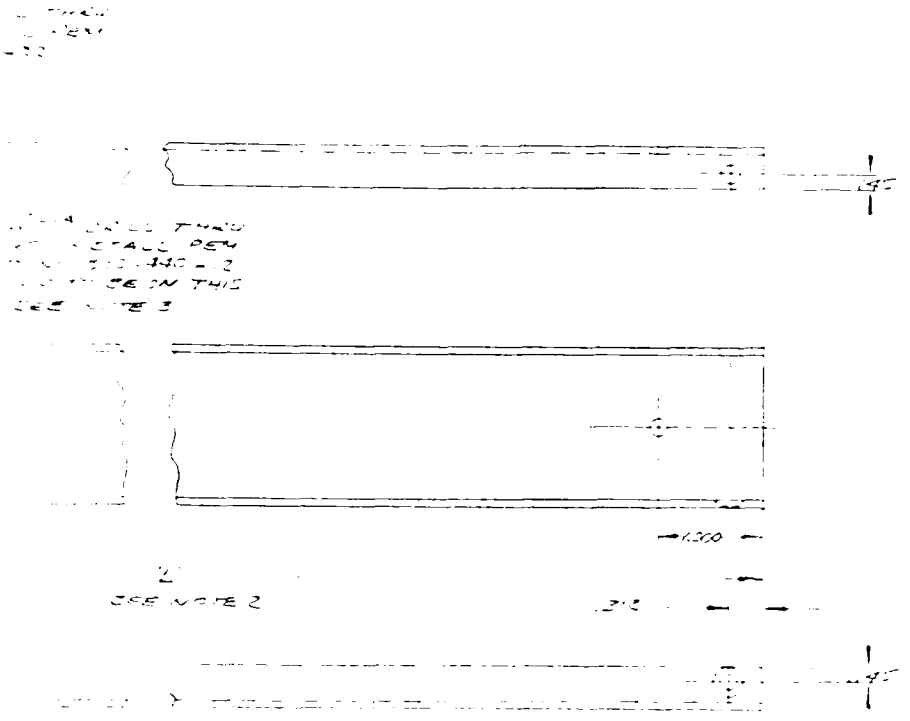
TITLE

SIZE DWG NO REV

SCALE SHEET OF


6
5
4
D
C
B
A
NO. 25 DRILL THRU C'SINK F
NO. 6 FLAT HEAD SCREW
FROM OTHER SIDE. 2 PLAC

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD



NOTES:
1. CAUSTIC ETCH & GOLD IRIDITE FINISH.
2. LENGTH L TO BE SPECIFIED PER NEED. [illegible]
3. HOLES AS SHOWN ON PIECES UP TO 6" L.
   - ADD CENTER HOLE ON PIECES WITH L 6" TO 9".
   - ADD TWO HOLES EQUAL SPACED BETWEEN THOSE SHOWN ON PIECES WITH L 15" TO 24".

ITEM	PART OR DWG. NO.	DESCRIPTION	QTY

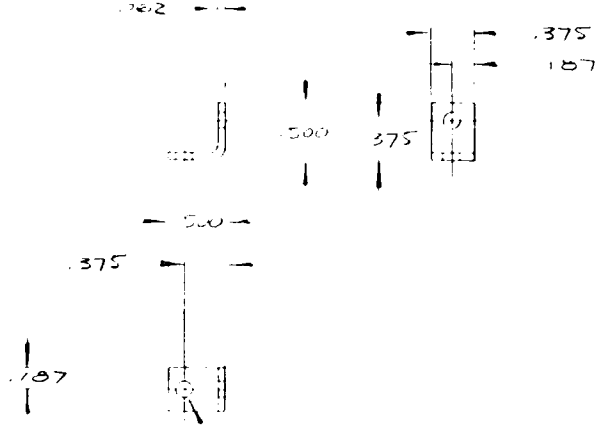
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. 10/82.06	WOODS HOLE OCEANOGRAPHIC INSTITUTION OCEAN ENGINEERING DEPT. WOODS HOLE, MA. 02543	
TOLERANCES: FRAC DECIMALS XX ± ANGLES ± XXX ±.005 — SURFACE MICRO IN ✓	APPROVALS / DATE DRAWN KDF 11-27-89 CHK'D APPVD	TITLE: CABLE RACE	
MATERIAL: 1/16 THICK 5052-H32 ALUMINUM	FINISH: SEE NOTE 1	SIZE C — DWG. NO. 00408 — REV.	
		SCALE FULL — SHEET OF	

D C A

DWG. NO.

REV.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD



-20-

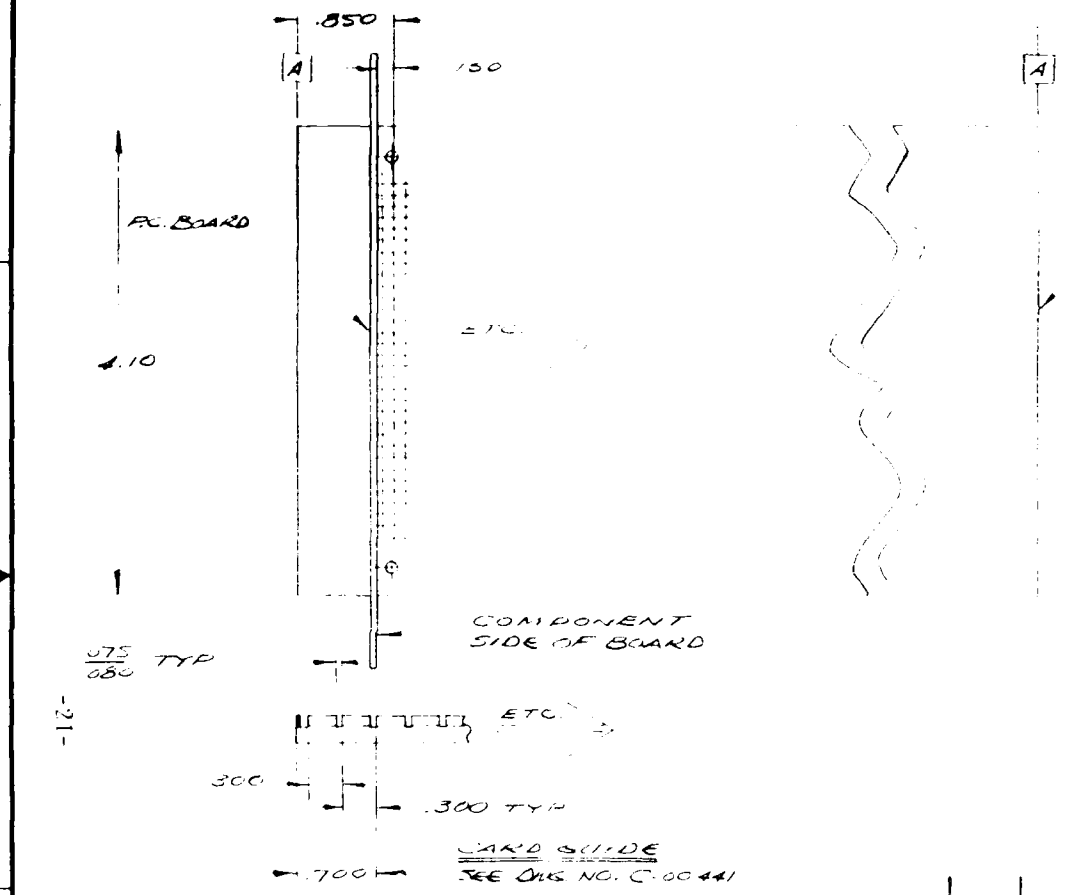
NO. 25 DRILL THRU, 2 PLACES

NOTES:
1. CAUSTIC ETCH & GOLD IRIDITE FINISH
2. PIECE MAY BE MADE FROM 1/2 x 1/2 x 1/16 ALUM. ANGLE.

ITEM	PART OR DWG. NO.	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRAC DECIMALS .XX ± .XXX ± .005 ANGLES ± SURFACE MICRO IN ✓	CONTRACT NO. 10/82 06	WOODS HOLE OCEANOGRAPHIC INSTITUTION OCEAN ENGINEERING DEPT. WOODS HOLE, MA. 02543	
	APPROVALS / DATE DRAWN KDF 11-27-89 CHK'D APPVD	TITLE BRACKET	
MATERIAL 5052-H32 ALUMINUM	FINISH SEE NOTE 1	SIZE B DWG. NO. 703905 REV. SCALE FULL SHEET OF	

MAREPEACE P 8078



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD

BACKPLANE P.C. BOARD

NOTES:
1. # OF CONNECTOR MIDDLE PIN ROWS ARE SPACED .300 APART.
2. SURFACE A IS FACE OF CHASSIS END PLATE. SEE DWG NO. C-00449
3. LENGTH OF BACKPLANE P.C. BOARD AND LENGTH OF CHASSIS TO BE DETERMINED FOR EACH APPLICATION

ITEM	PART OR DWG NO	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: FRAC DECIMALS ANGLES ° XX ± XXX ±
SURFACE MICRO IN ✓
MATERIAL

CONTRACT NO 10/82.06

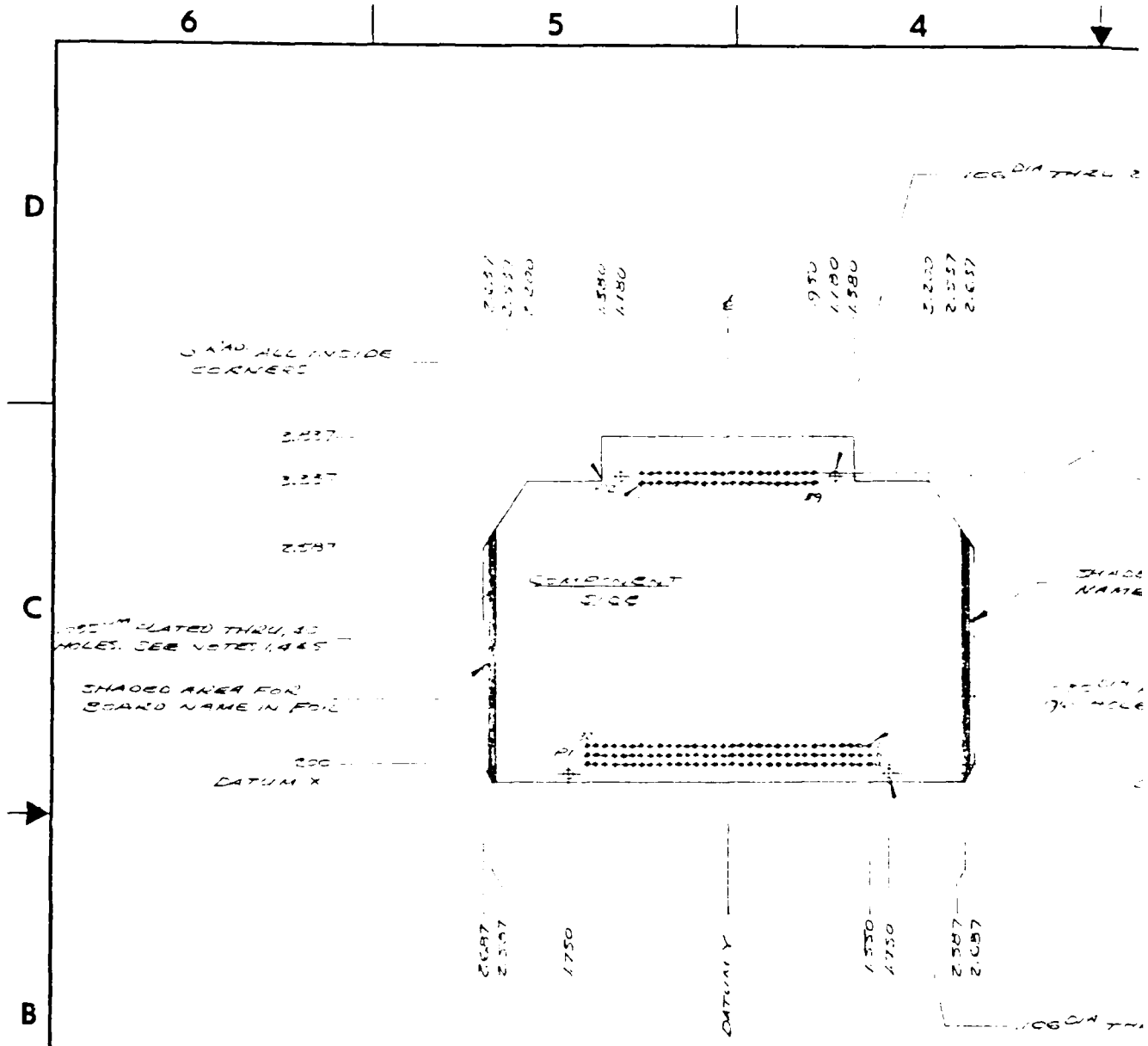
APPROVALS	DATE
DRAWN KDF	10/25/82
CHK'D	
APPVD	
FINISH	

WOODS HOLE OCEANOGRAPHIC INSTITUTION
OCEAN ENGINEERING DEPT.
WOODS HOLE, MA. 02543

TITLE: BACKPLANE P.C. BOARD AND CHASSIS RELATIONSHIP FOR ELECTRONIC CARD RACK ASY

SIZE B | DWG NO. 00884 | REV
SCALE | SHEET OF

MAKEPEACE # 6075



NOTES:
1. ALL PIN HOLES FOR CONNECTORS P1 & P2 TO BE POSITIONED ON .100" GRID PATTERN. TOLERANCES TO BE NON-CUMULATIVE.
2. VIEW SHOWN IS COMPONENT SIDE OF BOARD.
3. LABEL P1, COLUMN 1 & 32 AND ROWS a, b & c. WHEN P2 IS USED LABEL P2 & PINS 1 & 39.
4. IN SOME CASES, P2 HAS LESS THAN 40 PINS. THERE MAY ALSO BE TWO OR MORE SMALLER CONNECTORS IN THE P2 AREA.
5. DO NOT PLACE MOUNTING OR PIN SOLDER PADS ON BOARD WHEN P2 IS NOT USED. IN THESE CASES THE SPACE MAY BE USED FOR OTHER COMPONENTS.
6. BOARD PERIPHERY TO BE CUT TO DIMENSIONS SHOWN.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPVD

[illegible] THRU, 2 PLACES

.400
.750

PLACED AREA FOR BRAND NAME IN SILKSCREEN

[illegible] PLATED THRU HOLES SEE NOTE 1.

.250
.001
DATUM X

[illegible] THRU, 2 PLACES

ITEM	PART OR DWG. NO.	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES:
FRAC DECIMALS
ANGLES ± XX ± .XXX ± .005

SURFACE MICRO IN ✓

MATERIAL

CONTRACT NO 10/82.06

APPROVALS	DATE
DRAWN KDF	2/27/86
CHK'D	
APPVD	
FINISH	

WOODS HOLE OCEANOGRAPHIC INSTITUTION
OCEAN ENGINEERING DEPT.
WOODS HOLE, MA. 02543

TITLE
PRINTED CIRCUIT BOARD DIMENSIONS & LEGEND

SIZE C | DWG. NO. 00765 | REV.

SCALE FULL | SHEET OF

ON DWG
MS

COMPUTER BACKPLANE SPECIFICATION

3.1 Summary of Bus Operation

A functional description of bus operation is contained in Section 2 of IEEE Standard 796. The paragraphs below are intended to summarize the key features, by way of introduction for those unfamiliar with the bus.

Master/Slave Command/Acknowledge Sequence

Devices resident on the IEEE-796 bus are either masters or slaves. Masters control the bus; this includes acquiring access rights through bus arbitration and then generating bus control and address signals. Slaves are incapable of bus control; they respond to control and address signals from masters and accept or generate data in response. Master-slave data transfer is controlled by a simple asynchronous command/acknowledge handshake: the master issues an address followed by a command indicating the operation to be performed (read or write, I/O or memory); the addressed slave accepts or generates data as requested and issues an acknowledge signal (XACK*) which terminates the transaction. The command/acknowledge sequence is used for all data transfer across the bus, and also to transfer interrupt vectors during interrupt acknowledge proceedures.

Address, Data, and Control Busses

Signals on the IEEE-796 backplane are divided into address, data, and control groups. The address bus is driven by bus masters; the path width is 20 bits for memory addresses and 8 bits for I/O addresses. Both address and I/O spaces are addressed by byte, thus, the memory space is 1,048,576 bytes and the I/O space is 256 bytes. The data bus is a 16-bit bidirectional bus driven by either masters or slaves. Either 8-bit (byte) or 16-bit (word) data may be transferred, under the convention that byte data is always transferred on the low half (D0-D7) of the bus. This allows 8 and 16-bit devices to coexist on the same backplane. The control bus includes the command signals for memory and I/O read and write, the XACK acknowledge signal, clock, and reset.

Interrupts

There are eight prioritized interrupt request lines which can be activated by any slave desiring interrupt service. Masters may respond in one of two ways: for bus-vectored interrupts (BV) the master issues an interrupt acknowledge signal and receives an interrupt service vector from the bus, either from the requesting slave or from an interrupt controller. For non-bus-vectored interrupts all vectoring (if any) takes place internal to the master.

Bus Exchange

The bus exchange protocol allows more than one master to gain control of the bus, for example to allow two processors access to a global memory region. Both serial (daisy chain) and parallel arbitration techniques are defined; in the serial technique priority is established by physical location in the daisy

chain, while in the parallel method priority is resolved by a central priority module.

3.2 Bus Specification

Unless otherwise noted, IEEE-796 is the defining standard for the Instrument Bus computer backplane. The paragraphs below give the detailed specifications for the instrument-unique portions of the Instrument Bus backplane.

3.2.1 Changes from IEEE-796

In adapting IEEE-796 to the oceanographic instrument environment a number of changes were made to the IEEE standard, in order to reduce power consumption, increase the packaging density, and reduce circuit complexity. In addition, members of the 80C86 board set described in section 5 of this report deviate from the standard in a few key areas, in order to increase overall system data throughput. This section describes the changes made in converting IEEE-796 into the Instrument Bus, and also provides a cross reference to the non-compliant features of the board set described in section 5.

Summary of changes to IEEE-796:

1. Change board form factor, connector, and connector pinout (Table 2)
2. Change bus electrical specifications to CMOS (Section 3.2.3)
3. Limit I/O address to 8 bits; establish convention for I/O address assignments (Table 3)
4. Establish convention that Constant Clock (CCLK*) signal is derived from master (CPU) clock, and is not restricted to 10 MHz frequency.

Summary of 80C86 board set non-compliance:

1. 80C86 CPU:
   a) advanced Write commands
   b) CCLK disconnect capability
   c) First-INTA-XACK requirement
   d) Synchronous XACK

2. Memory and I/O bus interface circuit:
   a) advanced XACK

3.2.2 Bus Pinout

Pin assignments for the DIN 41612 Style C Instrument Bus connector are given in Table 2. Numeric pin numbers are provided in addition to the alphanumeric numbers used on the DIN connector. The "*" notation designates a signal which is low true (logic 1 when in the CMOS low state). The 18 unassigned pins, 27a through 32c, are available for any reasonable use. They are typically used for random wiring interconnection among boards plugged into the backplane.

TABLE 2
INSTRUMENT BUS PIN ASSIGNMENTS

Signal Group	Pin	Num	Signal	Description
Power Supply	1a-c	1-3	GND	Signal and Power Ground
	2a-c	4-6	+5V	+5V
	3a-c	7-9	+12V	+12V
	4a-c	10-12	GND	Signal and Power Ground
Bus Control	5a	13	BCLK*	bus clock
	5b	14	INIT*	initialize (reset)
	5c	15	BPRN*	bus priority in (non-bussed)
	6a	16	BPRO*	bus priority out (non-bussed)
	6b	17	BUSY*	bus busy
	6c	18	BREQ*	bus request (non-bussed)
	7a	19	MRDC*	memory read command
	7b	20	MWTC*	memory write command
	7c	21	IORC*	I/O read command
	8a	22	IOWC*	I/O write command
	8b	23	XACK*	transfer acknowledge
	8c	24	INH1*	inhibit 1 (disable RAM)
Bus Control/Address	9a	25	LOCK*	bus lock
	9b	26	INH2*	inhibit 2 (disable ROM)
	9c	27	BHEN*	bus high enable
	10a	28	A16*	address bit 16
	10b	29	CBRQ*	common bus request
	10c	30	A17*	address bit 17
	11a	31	CCLK*	constant clock
	11b	32	A18*	address bit 18
	11c	33	INTA*	interrupt acknowledge
	12a	34	A19*	address bit 19
Interrupt Request	12b	35	INT7*	interrupt request 7
	12c	36	INT6*	interrupt request 6
	13a	37	INT5*	interrupt request 5
	13b	38	INT4*	interrupt request 4
	13c	39	INT3*	interrupt request 3
	14a	40	INT2*	interrupt request 2
	14b	41	INT1*	interrupt request 1
	14c	42	INT0*	interrupt request 0
Address	15a	43	A15*	address bit 15
	15b	44	A14*	address bit 14
	15c	45	A13*	address bit 13
	16a	46	A12*	address bit 12
	16b	47	A11*	address bit 11
	16c	48	A10*	address bit 10
	17a	49	A9*	address bit 9
	17b	50	A8*	address bit 8

Signal Group	Pin	Num	Signal	Description
Address (continued)	17c	51	A7*	address bit 7
	18a	52	A6*	address bit 6
	18b	53	A5*	address bit 5
	18c	54	A4*	address bit 4
	19a	55	A3*	address bit 3
	19b	56	A2*	address bit 2
	19c	57	A1*	address bit 1
	20a	58	A0*	address bit 0
Data	20b	59	D15*	data bit 15
	20c	60	D14*	data bit 14
	21a	61	D13*	data bit 13
	21b	62	D12*	data bit 12
	21c	63	D11*	data bit 11
	22a	64	D10*	data bit 10
	22b	65	D9*	data bit 9
	22c	66	D8*	data bit 8
	23a	67	D7*	data bit 7
	23b	68	D6*	data bit 6
	23c	69	D5*	data bit 5
	24a	70	D4*	data bit 4
	24b	71	D3*	data bit 3
	24c	72	D2*	data bit 2
	25a	73	D1*	data bit 1
	25b	74	D0*	data bit 0
	25c	75		reserved
Power Supply	26a-c	76-78	GND	signal and power ground
Unassigned	27a thru 32c	79 thru 96		any board-specific use

3.2.3 Bus Drive Specification

The following specifications are intended to serve as a guideline for interfacing devices to the bus; they are typically based on the capability of the HC series of CMOS logic devices. At the system designer's discretion a reasonable degree of flexibility may be exercised, since application requirements vary over a wide range of speed/power tradeoffs. Bus line characteristic impedance and signal termination may be specified in the future for applications which require extreme speed.

Logic level requirements for Vdd = 5.0V, T(a) = -40 to +85 C:

signal level	receiver	driver
CMOS high state	5.5V > H > 3.5V	5.5V > H > 4.25V
CMOS low state	1.0V > L > -0.5V	0.36 > L > -0.5V

Bus Driver/Receiver Guidelines:

bus driver rated capacitive load	300	pF	min
bus driver tristate leakage	10	uA	max
input capacitance, per line, per board	20	pF	max
input leakage, per line, per board	3	uA	max
open collector pullup value	1.2	kohm	min
	10	kohm	max

3.2.4 I/O Address Convention

To reduce the parts count of I/O slaves, the IEEE-796 8-bit I/O address path option (compliance I8) is taken as standard for the Instrument Bus. The address assignments listed in Table 3 are recommended as a convention for the computer board set described in Section 5 of this report.

TABLE 3
I/O ADDRESS CONVENTION

address	board	function
00	Clock/Timebase	RTC counter -- milliseconds
01		RTC counter -- tenths and hundredths
02		RTC counter -- seconds
03		RTC counter -- minutes
04		RTC counter -- hours
05		RTC counter -- day of week
06		RTC counter -- day of month
07		RTC counter -- month
08		RTC RAM -- milliseconds
09		RTC RAM -- tenths and hundredths
0A		RTC RAM -- seconds
0B		RTC RAM -- minutes
0C		RTC RAM -- hours
0D		RTC RAM -- day of week
0E		RTC RAM -- day of month
0F		RTC RAM -- month
10		RTC interrupt status register
11		RTC interrupt control register
12		RTC counter reset
13		RTC RAM reset
14		RTC rollover status bit
15		RTC 'GO' command
16		RTC Standby Interrupt*
17		Clock Board - not used
18		Clock Board - not used
19		Clock Board - not used
1A		Clock Board - not used
1B		Clock Board - not used
1C		Clock Board - not used
1D		Clock Board - not used
1E		Clock Board - not used
1F		test mode
20	Serial I/O #1	Uart 1 (U7) Data
21		Uart 1 (U7) Control
22		Uart 1 (U7) Modem Control
23		Uart 1 (U7) Baud Rate select
24		Uart 2 (U6) Data
25		Uart 2 (U6) Control
26		Uart 2 (U6) Modem Control
27		Uart 2 (U6) Baud Rate select
28	Serial I/O #2	Uart 1 (U7) Data
29		Uart 1 (U7) Control
2A		Uart 1 (U7) Modem Control
2B		Uart 1 (U7) Baud Rate select
2C		Uart 2 (U6) Data
2D		Uart 2 (U6) Control
2E		Uart 2 (U6) Modem Control
2F		Uart 2 (U6) Baud Rate select

address	board	function
30	Parallel I/O #1	Port A Data
31		Port B Data
32		Port C Data
33		Mode Control
34	Parallel I/O #2	Port A Data
35		Port B Data
36		Port C Data
37		Mode Control
38	A/D Subsystem	read A/D low byte
39		read A/D high byte
3A		A/D status and control
3B		U2 mode control
3C		A/D start and Mux address
3D		spare (U3 port B)
3E		not used (U3 port C)
3F		U3 mode control
40	Counter/Timer	U8 Counter 0
41		U8 Counter 1
42		U8 Counter 2
43		U8 mode control
44		U9 Counter 0
45		U9 Counter 1
46		U9 Counter 2
47		U9 mode control
48		U10 Counter 0
49		U10 Counter 1
4A		U10 Counter 2
4B		U10 mode control
4C		U11 Counter 0
4D		U11 Counter 1
4E		U11 Counter 2
4F		U11 mode control
50	CPU Support and I/O	Latch Register (output) Switch Register (input) Deadman Reset (input)
51		not used
52		Interrupt Controller ICW1; OCW2,3
53		Interrupt Controller ICW2,3; OCW 1

IMPLEMENTATION AND DESIGN DESCRIPTIONS

4.1 Application and General Configuration

The initial application for the Instrument Bus concepts described in this report was the Schmitt-Toole Microstructure/Finescale Profiler [6]. This instrument required substantial computational throughput in order to perform simultaneous data acquisition (several kilobytes per second) and data analysis (spatial frequency estimation for adaptive sampling). To meet this requirement, the 80C86 processor family from Harris Semiconductor was selected for implementation of a computer board set based on the IEEE-796 backplane. The profiler also required a multichannel analog front end section, and a solid state mass storage subsystem based on CMOS static RAM. Implementation of the three separate electronic subsystems (analog, computer, and mass storage) provided a good opportunity to test and refine the Instrument Bus architecture.

A configuration diagram for the electronic systems of the Micro/Fine Profiler is shown in Figure 17. The Instrument Bus rack and packaging format was used for all three of the electronic subsystems. The analog front end contains several preamp/filter boards, power supplies, and an A/D converter. There is no analog "backplane" as such; rather, the board connectors are interconnected using point-to-point wiring. The computer contains the 80C86 board set, which is described in greater detail in Section 4.3 below; the configuration includes 128 kbytes of memory and the full set of I/O boards. The computer power requirement was 375 mW at 5V with the CPU operating at 5 MHz, and 7.5 mW with the CPU in Stop Oscillator mode. The mass storage subsystem [7] uses high density packaging techniques to place 1 Mbyte of CMOS static RAM on one 6" D card; four such cards make up the 4 Mbyte storage system. The mass store uses the same printed circuit backplane as the IEEE-796 computer system; however, the backplane signals were redefined and are unique to the mass storage application.

4.2 Design Descriptions, Schematics, and Parts Lists

This section includes detailed descriptions, schematics, and parts lists for each member of the 80C86 board set. The description of each board includes a brief summary of the board function, configuration instructions, application notes, and a detailed description of circuit operation. Since the I/O boards all share a common bus interface design, this circuit is described separately in section 4.2.1. For reference, Table 4 lists the board names, schematic and printed circuit artwork drawing numbers, and revision levels at the time of release of this report.

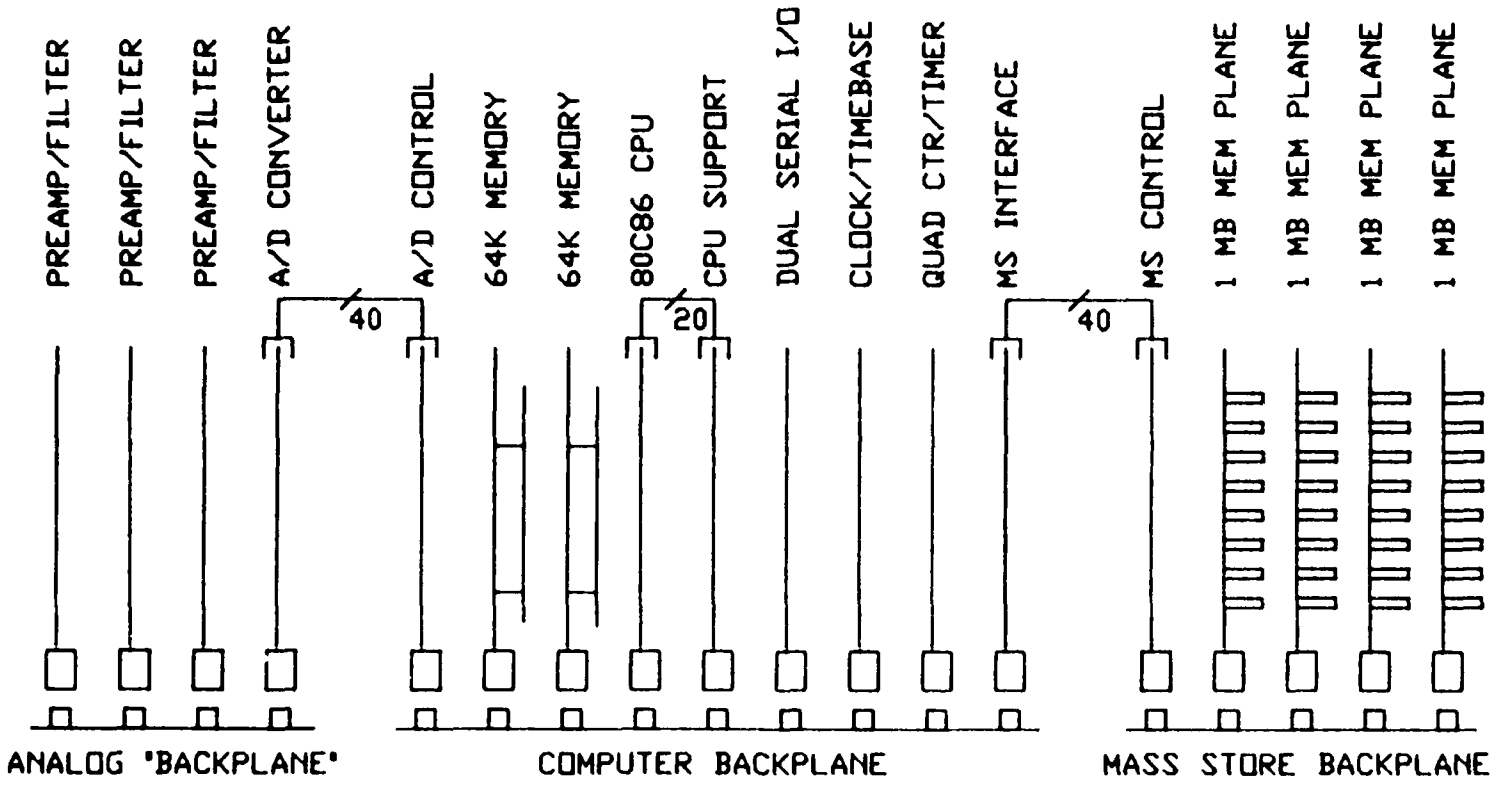


Figure 17
Micro/Fine Profiler Electronic Block Diagram

TABLE 4
INSTRUMENT BUS COMPUTER BOARD SET

board name	schematic	artwork	notes
80C86 CPU	00110	00111	rev A
CPU Support and I/O	00112	00113	rev A
Memory Control	00128	00129	
64k Memory Plane	00106	00202	
Dual Serial I/O	00101	00107	rev C
Parallel I/O	00102	00109	
Clock/Timebase	00103	00108	rev B
Quad Counter/Timer	00105	00105A	
9516 A/D Control	00122	00123	
9516 A/D Converter	00120	00121	
Terminator/Power Coupler	00114	00115	rev A

4.2.1 Standard I/O Interface Circuit

All of the I/O slaves (Serial, Parallel, Clock, Counter, A/D Converter) employ very similar circuits to interface to the IEEE-796 backplane. The operation of this circuit will be outlined using the Parallel I/O schematic. The other boards differ only in the details of decoding individual peripheral device chip selects.

On the Parallel I/O schematic (drawing 00102), U2 is a 74HC688 octal equality comparator. This device compares a board Base Address generated by Z1 with the address present on backplane address lines A2* - A7*; when all lines match, the P=Q output (ADET*) goes active (low). Ignoring address lines A0* and A1* causes U2 to decode a four-byte block of addresses; in general, the Base Address comparator will ignore one or more of the low-order address bits in order to decode the block of I/O addresses occupied by the peripheral devices on the board in question.

The ADET (or ADET*) signal indicates that a matching address is present on the address bus but does not indicate whether it is a memory or I/O address. An I/O operation on the backplane is signalled when one of the two I/O commands, IORC* (I/O Read) or IOWC* (I/O Write), goes active. These signals are ORed by negative-input OR gate U4A to generate the signal IOCMD, which indicates presence of an I/O command. Simultaneous occurrence of ADET and IOCMD indicates that an I/O operation is occurring to the board in question.

ADET and IOCMD are ANDed in parallel by two separate gates, U4D and U5C, in order to reduce access and response time. U4D, a conventional NAND gate, generates the enable signal to data bus transceiver U1. The transceiver normally drives "outward" (off the board, onto the backplane) unless the Write signal (IOWC*) is active. U5C, an Open Drain (OD) NAND, generates the XACK* signal which informs the bus master that the I/O address has been recognized and data is being output or accepted. The ADET* signal is used as the chip select (CS*) for U6, the 82C55 Parallel I/O port. U6 remains inactive until either RD* or WR* goes active as well, at which time A0 and A1 determine the function performed.

The I/O Interface circuit as described asserts the backplane XACK* handshake signal as soon as address decoding and command recognition are complete, even though valid data has not yet been output or accepted due to peripheral device access delays. This is a violation of IEEE-796 (paragraph 3.2.1, 3.2.2), but was done deliberately in order to avoid unnecessary wait states. All of the major 16-bit microprocessors (8086, 68000, 16032, 80286) perform external bus cycles in roughly similar fashion: an address is asserted and a command strobe (Read, Write, or Data) is activated; one clock cycle later a "Ready" handshake input is sampled and wait states are inserted until this signal is true; and finally Read data is latched or Write data is strobed one clock cycle after "Ready" is recognized. The immediate-XACK* circuit described above assures processor recognition of XACK* ("Ready") within one clock cycle of command assertion, avoiding extraneous wait states. The principal precaution required is to ensure that the peripheral chip access time will guarantee assertion (or acceptance) of valid data by the time the bus master requires it, usually the end of the second clock cycle. For the CPU types mentioned above, at clock rates of up to 8 MHz, the I/O boards described here should not experience any problems; but for higher speeds or other processor families the timing should be checked.

4.2.2 80C86 CPU

OE Dwg 00110
Revision: A Date: 24 July 1986 By: ecm

Description

The 80C86 CPU provides basic CPU and IEEE-796 Bus Master functions to Instrument Bus systems. The board contains the 80C86 chip itself, operated in Max Mode at up to 5 MHz; an 82C85 "stoppable" clock generator; 20 bits of address latch; 16 bits of data transceiver; and control and decoding logic to generate the basic IEEE-796 Command signals for Memory and I/O Read and Write. The board supports the IEEE-796 Byte Swap function, allowing it to work with 8-bit I/O devices. A 16-bit memory data path is required. Standing alone, the CPU board supports a single interrupt via the CPU Non Maskable Interrupt (NMI) input. For multiple interrupt sources, the CPU board also supports Bus Vectored interrupts, with the vector emitted onto the bus either by the CPU Support and I/O Board, or by a suitably equipped peripheral device.

The 80C86 CPU board is one member of a three-board set which implements a full-function IEEE-796 Bus Master. The other two boards are the CPU Support and I/O board, which provides an 82C59 8-input vectored interrupt controller along with a CPU "Deadman" timer and two 8-bit I/O ports; and the CPU DMA and Multimaster board, which provides a DMA controller and an 82C89 Bus Arbiter. The two or three board CPU set plugs into the Instrument Bus backplane, and is also interconnected by a private, 20-pin "frontplane" across the board top edges. As of this revision date the CPU and CPU Support boards have been designed and tested, while the DMA/Multimaster board has been defined but not yet implemented.

Configuration

Required for operation: Z2,Z3
Optional: Z1

Z1: Interrupt Select

The 80C86 CPU board has two interrupt inputs, the CPU Interrupt Request (INTR) and the CPU Non Maskable Interrupt (NMI) pins; and can accept interrupts from either of two sources, the backplane INT0* signal or the frontplane MINTR signal. Z1 allows either source to be connected to either input. Since the NMI input is self-vectoring, it can be used in small systems which lack a CPU Support board or other vectoring capability. In this case INT0* is used as the single interrupt request line, and a shunt plug installed at Z1-d connects this signal to the CPU NMI input. When a CPU Support and I/O board is available for interrupt vector generation, MINTR on the frontplane is connected to INTR on the CPU by installing a shunt at Z1-a. In this configuration, the backplane signal INT0* can also be connected, via Z1-d, to NMI on the CPU. The final configuration option is used when a peripheral device generates its own interrupt vectors; in which case INT0* from the backplane is used as the master interrupt request connected to the CPU INTR input via Z1-c.

Z2: Clock Source Select

The 80C86 CPU board uses a Harris 82C85 Static Clock Generator to provide the CPU clock signal. This device can operate with either an onboard oscillator, consisting of X1, C2, and C3; or from an "external frequency source" supplied to the EFI input pin. In either case the final CPU clock frequency is one-third of the input frequency. A shunt plug installed at Z2, which must be present for board operation, selects the Crystal or Frequency option.

Z3: Frequency Source Select

The 82C85 Clock Generator can accept an external frequency from two different sources. Z3, which must be present for operation, is used to select the frequency source, or to disable the EFI input when the Z2 "Crystal" option is selected. The frequency sources are either the EXCLK signal, supplied to the CPU board via uncommitted backplane pin 32a and selected by Z3a, or the 82C85 OSC output from the onboard crystal oscillator, selected by Z3b. The latter option is intended for use with the 82C85 Stop-Clock low power mode, as described in the Application section below.

Application Notes

The 80C86 CPU board allows two different methods of stopping the CPU clock in order to reduce system energy consumption. Both are implemented by the 82C85 Clock Generator; they are entered transparently by execution of the 8086 instruction HALT and exited (CPU restarted) upon occurrence of any interrupt. The lowest power (essentially static drain) standby mode is Stop-Oscillator, which disables the 82C85 crystal oscillator circuit. This mode is enabled by selecting the Crystal option using Z2. The principal drawback of this mode is the time required for restart, which will be of order Q+8000 clock cycles, where Q is the crystal Q. The fastest reponse (a few clock cycles) standby mode is Stop-Clock, which disables the CPU CLK signal but leaves the local oscillator running. This mode is enabled by selecting the Frequency option using Z2, and selecting either the OSC or EXCLK frequency source (The 82C85 oscillator does not stop when the Frequency option has been selected). The principal drawback with this mode is the oscillator standby power, which is approximately 1 mA per MHz of crystal frequency.

The 80C86 CPU is compliant with all relevant specifications of IEEE-796, with the exceptions noted below. For information, computed values of key timing requirements from the standard (Section 3.2) are listed below. The formulae are based on timing specifications from the 80C86 data sheet, with a 5 MHz CPU clock assumed.

name	symbol	value		formula	
address setup	t(AS)	60	ns	TCLCL - TCLAV + TCLML - TPD	
address hold	t(AH)	235	ns	TCLCL + TCLLH/2 + TSHOV/2	
command width	t(CMD)	400	ns	2 x TCLCL	
command hold	t(CMPH)	240	ns	TR1VCL + TCLCL + TCLMH	
command sep'n	t(CSEP)	400	ns	2 x TCLCL	
INTA* width	t(INTA)	400	ns	2 x TCLCL	
data setup (1)	t(DS)	-140	ns	TCLML - TCLDV - TIVOV	(note 1)
data setup (2)	t(DS)	250	ns	2 x TCLCL - TCLDV - TIVOV - TCLMH	
data hold	t(DH)	110	ns	TCLCH - TCLMH + TCHDX + TIVOV/2	

note 1: (1) is data setup to leading edge of MWTC* or IOWC*,
(2) is data setup to trailing edge of MWTC* or IOWC*

Compliance Notation:

80C86 CPU (standalone): Master D16,M20,I8,V0
80C86 CPU (with CPU Support): Master D16, M20, I8, V02

Compliance Exceptions:

The four points described below are the known areas of non-compliance with IEEE-796.

1. Advanced Write Commands The 82C88 "advanced" write commands AMWTC* and AIOWC* are used to generate the backplane commands MWTC* and IOWC*. This approach allows slave devices to generate XACK* during the CPU T2 clock cycle, thus avoiding unnecessary wait states. Slaves which latch Write data on the trailing edge of MWTC* or IOWC* will function correctly. Formally, these advanced commands are in violation of IEEE-796 (paragraph 3.2.2); systems including slaves which cannot tolerate a negative data setup time to the MWTC* or IOWC* leading edge should use the regular 82C88 Write outputs.

2. CCLK* Disconnect Capability No provision has been made for disconnection of CCLK* in multimaster systems (paragraph 2.1.3.1.1). This capability will be added at whatever future date multimaster capability is added to the CPU Group board set.

3. First-INTA-XACK The circuit which generates XACK* during the first INTA* cycle of an interrupt sequence as required by IEEE-796 (paragraph 3.2.4.2), is located on the CPU Support board, as is the circuit which generates the EA0 data buffer control signal. This prevents a standalone CPU board from accepting interrupt vectors from the bus.

4. Synchronous XACK* The 82C85/80C86 specifications for "Ready" inputs RDY and AEN* require single-stage synchronization for signals synchronous with CLK, and two-stage synchronization for asynchronous signals. Two-stage synchronization, which would be needed for a canonical IEEE-796 implementation, requires slaves to return XACK* within 48 ns of worst-case command activation in order to avoid a wait state; this is less than two HCMOS gate delays and places severe constraints on design of the slave. Since most slaves (specifically those based on the Standard I/O interface) return XACK* synchronous with the commands and with CCLK*, single-stage synchronization was selected for the CPU board; this allows an additional 68 nsec for slave response and generally allows unneeded wait states to be

avoided. Systems with asynchronous XACK* signals can change 82C85 modes by pulling the ASYNC* pin (U8 pin 21) low if required.

Circuit Description

The 80C86 CPU board consists of the following subsections: the CPU itself, CPU clock generator, backplane interfaces to the address, data, and command busses, and the frontplane expansion connector. In general, the design is straightforward and the circuit operation can be deduced from the schematic. Additional notes on each of the subsections are provided below.

U1 is the 80C86 CPU itself. It is operated in Max Mode to allow use of the 80(C)87 coprocessor. The LOCK* and RQ/GT0* signals are made available on the frontplane (via P2) for use by additional coprocessors, or by the 80C89 Bus Arbiter. U8 generates the CPU clock and synchronizes the READY and RESET signals to the CPU; the CLK output is heavily buffered by U2C and D for driving the backplane CCLK* signal. S1, U2F, and Q1 provide an onboard pushbutton Reset and INIT* function. U3C and D detect the application of any interrupt to the CPU and "wake up" the clock generator if it is in STOP mode. U9 decodes the CPU Status outputs and generates the backplane Command signals. The frontplane AEN* signal is generated by the 82C89 on the Multimaster board and is merely pulled true on the CPU board; when negated (driven high) it forces the CPU into a wait state and disables the CPU board address and command bus drivers.

The address bus drivers are U10,11,and 12; the 82C83 devices were chosen for their 300pF drive capability. When a CPU Support board is present, an interrupt cascade code is generated by the 82C59 Interrupt Controller on that board; this code is gated (by the MCE signal) over the frontplane onto address/data lines AD8-AD10 during interrupt acknowledge cycles. Similarly, a special A0 signal (EA0) from the CPU Support board conditions the CPU board data transceivers to receive an interrupt vector on the low byte of the data bus during interrupt acknowledge.

The data bus transceivers are U5,6, and 7, again chosen for 300 pF drive capability, plus associated control logic U4 and U13. U13 latches the CPU A0 and BHE signals; U4 decodes these signals for data bus control. To paraphrase IEEE-796 paragraph 2.2.2.4, D0-D7 are used for odd or even byte transfers, and D0-D15 are used (with BHEN* asserted) for word transfers; D8-D15 are used only for the high byte of word transfers. The following truth table summarizes transceiver and data bus operation:

A0	BHE	BHEN	Xcvr Enabled	Operation
0	0	0	low	even-address byte on D0-D7
0	1	1	low+high	even-address word on D0-D15
1	1	0	swap	odd-address byte on D0-D7
1	0			not used

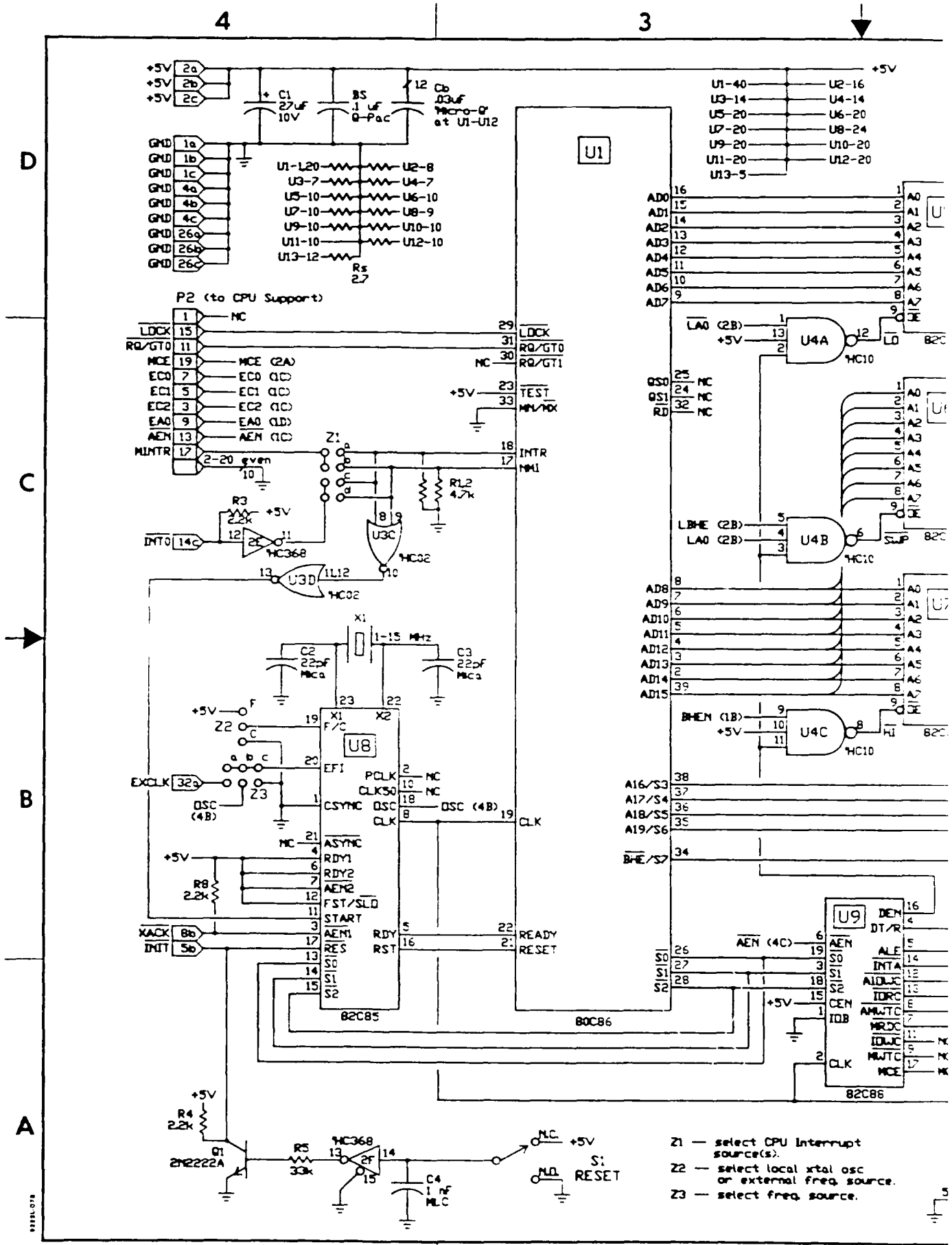
These conventions allow the 80C86 CPU board to access 8-bit peripherals, and also allow 8-bit CPU boards (masters) to access 16-bit memory and I/O boards (slaves).

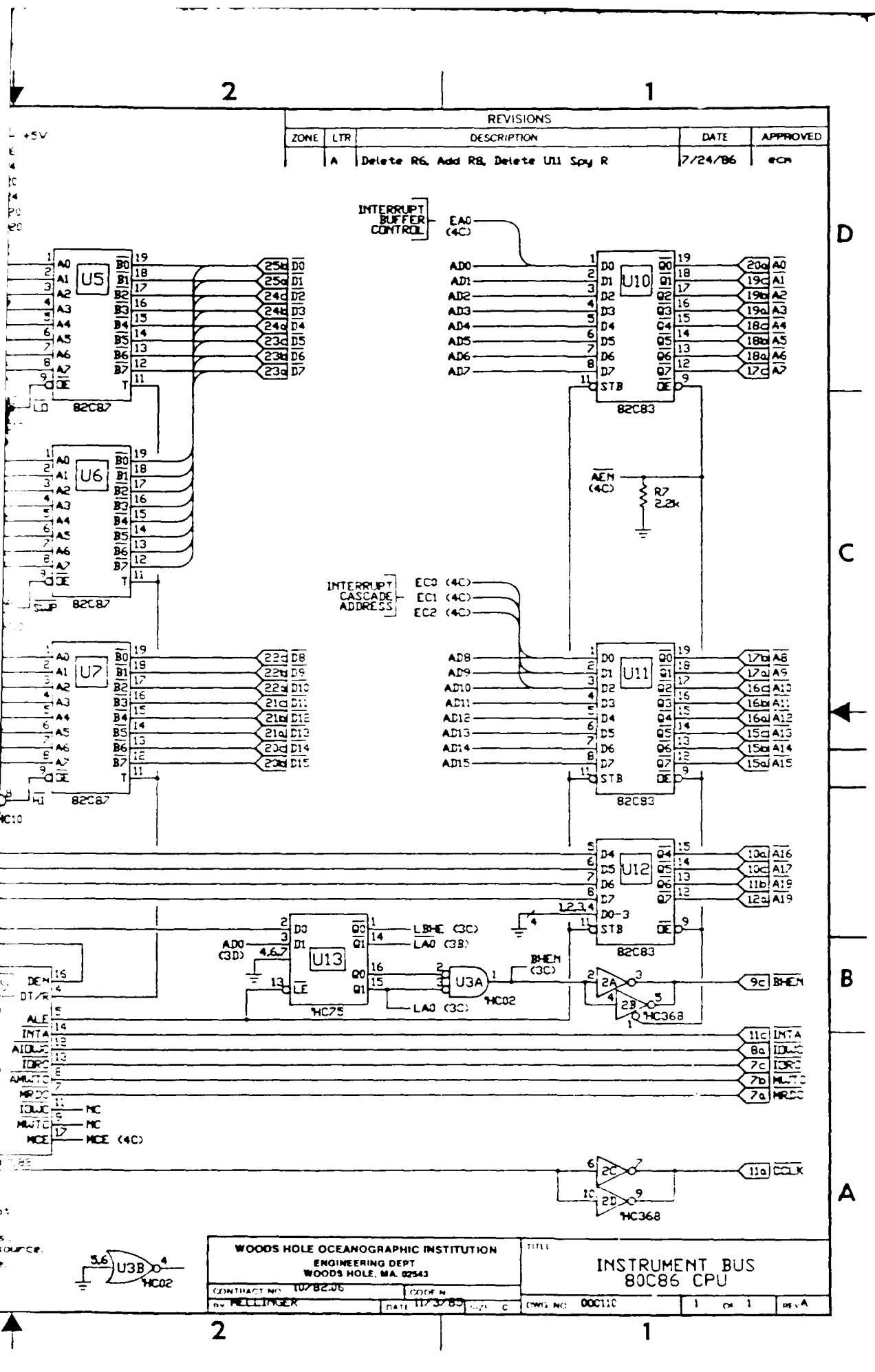
U13 is the source of the only currently known timing problem on the CPU board: at 5 MHz, a worst-case clock-to-BHE* time of 110 nsec coupled with a worst-case clock-to-ALE time of 4 nsec would violate the 74HC75 data-to-clock

setup requirement (25 nsec) by 13 nsec. This is unlikely to occur since the 80C86 BHE* output is specified for 100 pF and is only driving 10 pF, but it is a potential problem area which should be monitored during production checkout. Experience to date indicates an average clock-to-BHE* time of 45 +/- 10 nsec.

The following minor circuit changes are planned for future revisions of the 80C86 CPU board:

1) Disconnect for CCLK* signal
2) Enable 82C85 READY with board AEN* signal
3) Shunt plug to strap 82C85 ASYNC* input low
4) Shunt plugs to select Advanced or Normal Write Commands.
5) Connect P2 pin 1 to 82C85 FST/SLO* input for clock speed control


4
3
D
C
B
A
U1
80C86
U8
82C85
U9
82C86
P2 (to CPU Support)
U4A
U4B
U4C
U3C
U3D
HC10
HC32
HC368
Z1 — select CPU interrupt source(s).
Z2 — select local xtal osc or external freq. source.
Z3 — select freq. source.


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | Delete R6, Add R8, Delete U11 Spy R | 7/24/86 | ecn
INTERRUPT BUFFER CONTROL
EA0 (4C)
INTERRUPT CASCADE ADDRESS
EC0 (4C)
EC1 (4C)
EC2 (4C)
AEN (4C)
R7 2.2k
U5
U6
U7
U10
U11
U12
U13
82C87
82C83
HC75
HC02
HC368
U3A
U3B
LBHE (3C)
LA0 (3B)
LA0 (3C)
BHEN (3C)
ALE
INTA
MCE (4C)
COLK
WOODS HOLE OCEANOGRAPHIC INSTITUTION
ENGINEERING DEPT
WOODS HOLE, MA. 02543
INSTRUMENT BUS
80C86 CPU
DWG NO 000110
REV A

Instrument Bus
80C86 CPU
CE Dwg. 00110

Rev A 24 July 1986 ecm

Designation	Quan	Value	Rating	Type	Mfgr and Part Number
R1,2	2	4.7k	1/4W	5% Carbon Film	
R3,4,7,8	4	2.2k	1/4W	"	
R5	1	33k	1/4W	"	
R6	0	(not used)			
R9	12	2.7	1/8W	Carbon Comp	Allen-Bradley 'BB'
C1	1	27uF	10V	Solid Tantalum	CSR13-M39003/01-2496 (Sprague)
C2,3	2	22pF		Silver Mica	
C4	1	1nF	50V	CK05 Ceramic	
C5	2	20nF	14 pin	Micro-Q	Rogers uQ-14.02
C5	1	30nF	16 pin	"	Rogers uQ-16.03
C5	1	30nF	18 pin	"	Rogers uQ-18.03
C5	7	30nF	20 pin	"	Rogers uQ-20.03
C5	1	70nF	40 pin	"	Rogers uQ-40.07
Q1	1	2N2222A			
X1	1	1-15 MHz	AT-Cut	HC-18 Holder	(frequency as required)
U1	1	80C86	16 Bit CPU		Harris ID-80C86
U2	1	74HC368	Hex Tristate Inverter		Mot. 74HC368J (DS)
U3	1	74HC02	Quad NOR		Mot. 74HC02J (DS)
U4	1	74HC10	Triple NAND		Mot. 74HC10J (DS)
U5,6,7	3	82C87	Octal Inverting Transceiver		Harris ID-82C87
U8	1	82C85	Static Clock Generator		Harris ID-82C85
U9	1	82C88	Bus Controller		Harris ID-82C88
U10,11,12	3	82C83	Octal Inverting Latch		Harris ID-82C83
U13	1	74HC75	Dual D Latch		Mot. 74HC75J (DS)
S1	1		SPDT Pushbutton		C&K 8121-D9-AC
P1	1		DIN Connector		STV-C 96-M-abc ERNI 533-402
P2	1		AmpLatch 20		AMP 102326-4
J1-5	17		Shunt/Wrap Post		Samtec TSW-136-07-G-S
	4		Shunt		AMP 530153-2

4.2.3 CPU Support and I/O

OE Dwg 00112
Revision: A Date: 3 October 1985 By ecm

Description

The CPU Support and I/O board provides a number of auxiliary functions to the 80C86 CPU board. An 82C59A Interrupt Controller supports the eight interrupt request signals on the IEEE-796 backplane, and can either emit its own vectoring information or work in cascade mode with peripherals capable of bus vectored operation. A CPU "Deadman" circuit can be configured to detect the absence of regularly scheduled CPU activity, and either interrupt or reset the CPU. Two general purpose parallel I/O ports, a "switch register" for input and a "latch register" for output, are available for miscellaneous parallel or bitwise control functions in small systems. The CPU Support board is the second member of the CPU Group board set, which also includes the 80C86 CPU, and the DMA and Multimaster board.

Configuration

Required for operation: Z1
Optional: Z2,3,4,5,6

Z1: Base Address

The CPU Support board occupies 4 locations in the IEEE-796 I/O address space. Z1 selects the board base address in this space; all six shunt plugs must be installed for correct operation. The 4 locations have the following assignments:

Base + 0	Latch Register (output)
	Switch Register (input)
	Deadman Reset (input)
Base + 1	not used; duplicate of Base+0
Base + 2	Interrupt Controller ICW1; OCW2,3
Base + 3	Interrupt Controller ICW2,3; OCW 1

Z2: Deadman Interrupt Enable

Halfway through the programmed deadman time the deadman counter (U6) generates the DMI* Deadman Interrupt signal. Z2 is used to enable this signal onto backplane interrupt request line INT0*, where it can generate an interrupt either through the 82C59 controller or through the NMI* non-maskable interrupt on the CPU board.

Z3: Switch Register Input

U12 is an 8-bit input port which can either be used as a dipswitch register for reading configuration information, or as a regular input port by reading digital inputs supplied through connector P3. Z3 is used to configure these functions, either through installation of shunt plugs

to tie input lines high or low, or through wire-wrap connection of the center post row (the input row) to P3 via Z5.

Z4: Latch Register Output

U11 is an 8-bit latched output port which can be wire-wrap connected to connector P3 via Z4 and Z5.

Z5: Uncommitted Input/Output

Z5 provides 8 uncommitted I/O lines via AmpModU connector P3. These can be connected to either the Switch Register inputs or the Latch Register outputs by wire-wrap, as required by application.

Z6: Deadman Reset Enable

A shunt plug installed at Z6 will enable deadman timer U6 to reset the computer system on timeout, by pulling the backplane INIT* signal low.

Application Notes

The deadman timer is programmed for the desired deadman timeout time by selection of oscillator component values for Rf, Rx, and Cx. This RC oscillator is subject to drift over temperature and time, and should not be used for precision timing generation. An approximate formula for the deadman timeout (time from deadman reset until deadman activates INIT* signal) is:

Deadman Timeout = 18,000 x (RxCx) seconds

where Rx is in ohms and Cx is in Farads. The value of Rf should be chosen to be roughly five times the value of Rx, and should also be kept to less than a few megohms maximum.

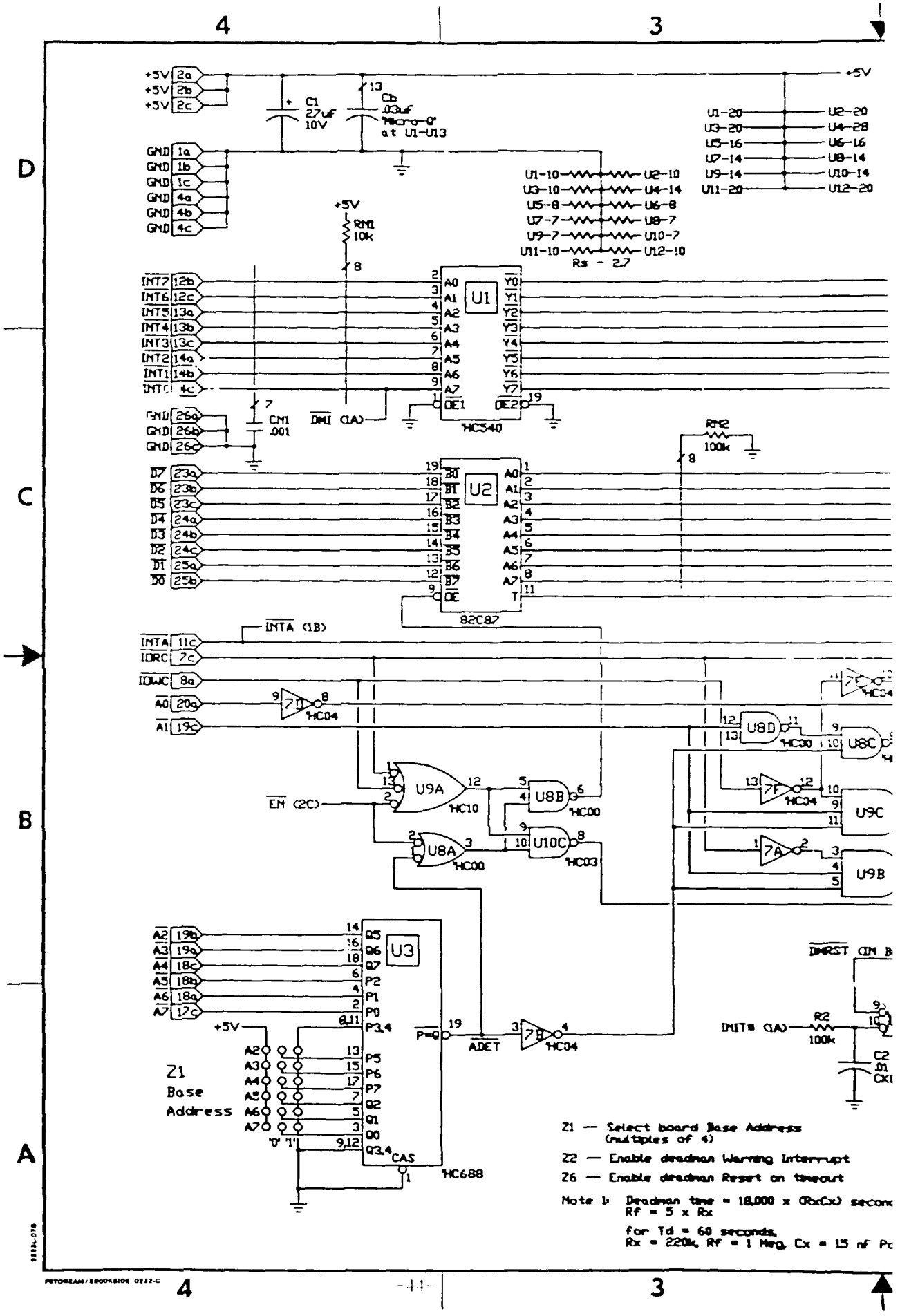
Compliance Notation:
Slave D8, I8, V02

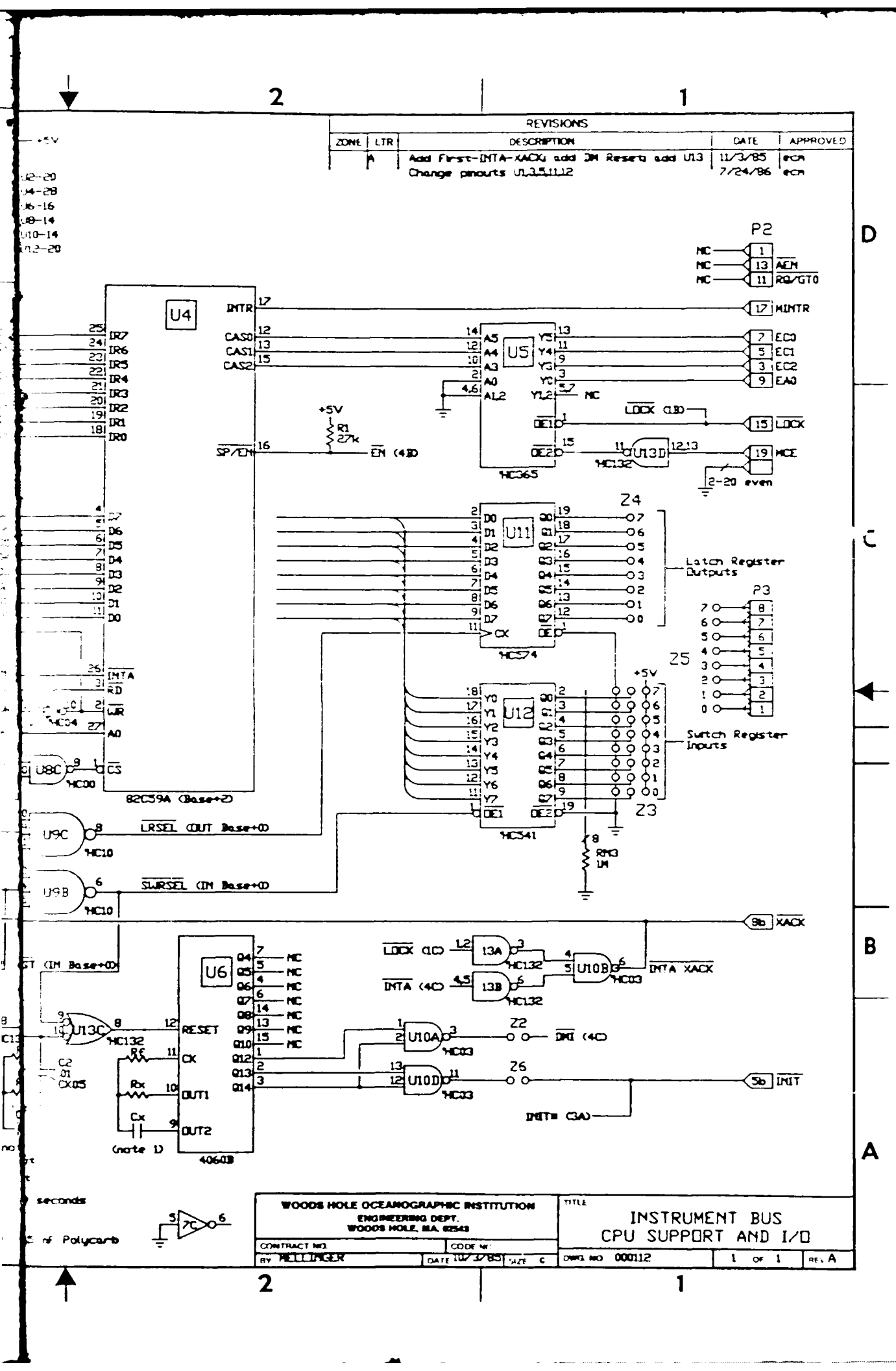
Circuit Description

The standard I/O interface, U2,3,7,8,9, and 10, is augmented by the inclusion of the EN* (Enable) signal in the generation of IOCMD at U9A. This allows interrupt controller U4 to enable data transceiver U2 for emission of the interrupt type code, and to generate XACK, during the second INTA cycle of an interrupt response. For normal I/O, the function of the standard I/O interface is effectively unchanged. U13A,B and U10B decode status signals from the CPU to generate XACK during the first INTA cycle.

An input operation from the Switch Register performs the dual function of reading the register via buffer U12, and resetting the Deadman counter U6. U6 can also be reset by an externally asserted INIT* signal on the backplane, as from the CPU RESET pushbutton; or by its own activation of the INIT* signal. In the latter case, RC network R2-C2 and Schmitt trigger U13C are used to "stretch" the width of the INIT* pulse.

The interrupt cascade address generated by interrupt controller U4 is gated onto the frontplane, and thence to the CPU board, by buffer U5 in response to the CPU LOCK* and MCE signals. U1 is used to buffer and invert the backplane interrupt request signals INT0*-INT7*. Capacitor network CN1 was added to reduce the amplitude of crosstalk noise on the open-drain interrupt request signals after capacitive coupling problems were experienced between A19* and INT7* on the backplane. This (somewhat hamfisted) fix should not be required once a shielded multilayer backplane is available.


4
3
D
C
B
A
+5V
GND
C1
27uF
10V
Cb
.03uF
Macro-0
at U1-U13
RM1
10k
Rs - 27
U1-10 U2-10
U3-10 U4-14
U5-8 U6-8
U7-7 U8-7
U9-7 U10-7
U11-10 U12-10
U1-20 U2-20
U3-20 U4-28
U5-16 U6-16
U7-14 U8-14
U9-14 U10-14
U11-20 U12-20
INT7 INT6 INT5 INT4 INT3 INT2 INT1 INT0
U1
HC540
CM1
.001
DMI (1A)
RM2
100k
D7 D6 D5 D4 D3 D2 D1 D0
U2
82C87
INTA (1B)
INTA IORC IOWC A0 A1
HC04
EN (2C)
U9A
U8B
U8A
U10C
U8D
U8C
U9C
U9B
HC10
HC00
HC03
HC30
A2 A3 A4 A5 A6 A7
U3
P=0
ADET
HC688
Z1
Base
Address
CAS
DMRST (2M B
INIT= (1A)
R2
100k
Z1 — Select board Base Address
(multiples of 4)
Z2 — Enable deadman Warning Interrupt
Z6 — Enable deadman Reset on timeout
Note 1: Deadman time = 18,000 x (RxCx) secon
Rf = 5 x Rx
for Td = 60 seconds,
Rx = 220k, Rf = 1 Meg, Cx = 15 nF Pc


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | Add First-INTA-XACK; add 2M Resets add U13 | 11/3/85 | ecm
Change pinouts U1,3,5,11,12 | 7/24/86 | ecm
P2
P3
U4
U5
U6
U8C
U9B
U9C
U10A
U10B
U10D
U11
U12
U13A
U13B
U13C
U13D
82C59A (Base+20)
HC574
HC541
HC365
HC132
HC00
HC10
HC03
HC04
4060B
INTR
MINTR
LOCK
MCE
EN (43D
LRSEL (OUT Base+0D
SLVRSEL (IN Base+0D
INTA XACK
INIT
Latch Register Outputs
Switch Register Inputs
Z2
Z3
Z4
Z5
Z6
R1 27k
RP3 1M
R6
Rx
Cx
C2 .01 CK05
(note 1)
seconds
of Polycarb
WOODS HOLE OCEANOGRAPHIC INSTITUTION
ENGINEERING DEPT.
WOODS HOLE, MA. 02543
TITLE
INSTRUMENT BUS
CPU SUPPORT AND I/O
BY MELLINGER
DATE 10/3/85
SIZE C
DWG NO 000112
1 OF 1
REV A

Instrument Bus
CPU Support and I/O
CE Dwg. 60112

1 of 1

Rev A 3 Nov 1985 ecm

Designation	Quan	Value	Rating	Type	Mfgr and Part Number
R1	1	27k	1/4W	5% Carbon Film	
R2	1	100k	1/4W	5% Carbon Film	
Rx	1	see note		1% RN55	(select for desired Deadman time)
Rf	1	see note		1% RN55	(select for desired Deadman time)
Rs	13	2.7	1/8W	Carbon Comp	Allen-Bradley 'BB'
RN1	1	10k x 9		SIP Network	Dale MSP10A01-103G
RN2	1	100k x 9		SIP Network	Dale MSP10A01-104G
RN3	1	1M x 9		SIP Network	Dale MSP10A01-105G
C1	1	27uF	10V	Solid Tantalum	CSR13-M39003/01-2496 (Sprague)
C2	1	10nF	50V	CK05 Ceramic	
Cx	1	see note		Stacked Film	(select for desired Deadman time)
CN1	1	1nF x 7		SIP Network	Sprague 470C7X7R-102K5DG
Cb	4	20nF	14 pin	Micro-Q	Rogers uQ-14.02
Cb	2	30nF	16 pin	Micro-Q	Rogers uQ-16.03
Cb	5	30nF	20 pin	Micro-Q	Rogers uQ-20.03
Cb	1	30nF	28 pin	Micro-Q	Rogers uQ-28.03
U1	1	74HC540	Octal Inverting Buffer		Mot. 74HC540J (DS)
U2	1	82C87	Octal Inverting Transceiver		Harris ID-82C87
U3	1	74HC688	Octal Comparator		Mot. 74HC688J (DS)
U4	1	82C59A	Interrupt Controller		Harris ID-82C59A
U5	1	74HC365	Hex Tristate Buffer		Mot. 74HC365J (DS)
U6	1	4060B	Oscillator/Divider		RCA CD4060BF (XV)
U7	1	74HC04	Hex Inverter		Mot. 74HC04J (DS)
U8	1	74HC00	Quad NAND		Mot. 74HC00J (DS)
U9	1	74HC10	Triple NAND		Mot. 74HC10J (DS)
U10	1	74HC03	Quad NAND OD		Mot. 74HC03J (DS)
U11	1	74HC574	Octal D Flip-Flop		Mot. 74HC574J (DS)
U12	1	74HC541	Octal Buffer		Mot. 74HC541J (DS)
U13	1	74HC132	Quad Schmitt NAND		Mot. 74HC132J (DS)
P1	1	DIN Connector STV-C 96-M-abc			ERNI 533-402
P2	1	AmpLatch 20			AMP 102326-4
P3	1	AmpModU 8			AMP 3-87516-4
Z1-6	62	Shunt/Wrap Post			Samtec TSW-136-07-G-S
	16	Shunt			AMP 530153-2

4.2.4 Memory Control

OE Dwg 00128
Revision: none Date: 3 November 1985 By: ecm

Description

The Memory Control board provides program and data memory capability for Instrument Multibus systems. In combination with a 64 or 256 kbyte Memory Plane, a Memory Module is formed which supports 20-bit addresses and 8 or 16 bit data paths.

Configuration

Required for operation: Z1,Z2,Z3,Z4,Z5,Z6
Optional: none

Z1: Memory Device Address Gate Enable

Backplane address signals A0*-A15* are buffered to the eight memory devices on the Memory Plane by transparent latches U1 and U2, which are normally operated in transparent (latch not enabled) mode. In multiple-memory-module systems, the energy expense of driving 128 device inputs through each address transition can be eliminated by only driving the address on the module which is selected during a particular bus cycle. This is done with Z1 on the Memory Control board by connecting the Latch Enable (LE*) inputs to ADET, the board address signal from U3. This conditions U1 and U2 to be transparent (i.e. to drive the backplane address to the memory devices) only when the board base address has been detected (ADET true); U1 and U2 are latched at all other times. A shunt plug must be installed at Z1 for proper board operation; it should be connected to +5V (Z1b-c) to disable the address gating described above, or to ADET (Z1a-b) to enable address gating. Address gating reduces the available memory device address-to-data access time by the propagation delay through the ADET logic, which is 76 nsec worst case.

Z2: Chip Select Gate Enable

Chip select signals for memory devices on the Memory Plane are normally decoded from a selected subset of the backplane address signals by U4 and U5. Decoding and chip selection are active regardless of whether the bus cycle is a memory operation, an I/O operation, or an idle cycle. Since power consumption for most bytewide memory devices is much higher when chip select is active, Z2 is provided to allow the chip selects to be enabled (gated) only when a memory cycle is in progress. A shunt plug must be installed at Z2 for proper board operation. Connecting the shunt to MEMCMD (Z2a-b) will enable chip select gating, while connecting the shunt to +5V (Z2b-c) will disable gating. Chip select gating reduces the available memory device select-to-data time by the difference between the master's address-valid and command-valid times, plus 21 nsec (a minimum of 71 nsec).

Z3: Base Address

The Memory Module of which the Memory Control board is a part occupies either 64k or 256k byte locations in the IEEE-796 memory address space. Z3 selects the module base address within this memory space. Four shunt plugs must be installed at Z3 for proper board operation; for 256k memory planes, the shunts for A16 and A17 must be installed on the '1' side of the jumper field..

Z4: Memory Plane Size/Decoder Inputs

The inputs to chip select decoders U4 and U5 must be derived from address signals appropriate for the memory plane size in use. Z4 is used to perform this selection; one shunt plug must be installed at each of Z4A and Z4B for proper operation. Shunting the 'a' rows will produce chip selects for 64k planes, while shunting the 'c' rows will produce selects for 256k planes. The 'b' row is for 128k planes, an obsolete size which is unlikely to be implemented.

Z5: Memory Plane Size/Comparator Inputs

The inputs to base address comparator U3 must similarly be derived from address lines appropriate for the memory plane size in use. In particular, the function of A16 and A17 changes depending upon whether the memory module occupies 64k or 256k of memory space. Z5 performs this selection function; two shunt plugs are required for proper operation. Rows 'a' and 'b' should be shunted for use with 64k memory planes, while rows 'b' and 'c' should be shunted for 256k planes.

Z6: Single Board Operation

Instrument Bus systems with just one memory board may find it useful to disable base address comparator U3 by forcing ADET* true, either to speed access times or to telescope the system address space into one board. (The latter feature is applicable to 8086-based systems, which require interrupt vectors at one end of the address space and a reset jump vector at the other end.) A shunt plug must be installed at Z6 for proper operation. Connect the shunt to ADET* ('a' and 'b') for normal multi-board operation; connect it to ground ('b' and 'c') for single-board operation.

Application Notes

Assuming that Z1 and Z2 are configured for full speed operation (no address or chip select gating), the Memory Module has the following worst case access and response time characteristics:

Access, address-to-data:	67 nsec plus memory device address-to-data time
or	117 nsec plus memory device select-to-data time
Access, command-to-data:	59 nsec plus memory device RD/WR-to-data time
Response, command-to-XACK:	13 nsec min, 55 nsec max (see note)

note: The Memory Control board employs a bus interface circuit which is similar to the standard I/O interface circuit. As discussed in the description of the I/O circuit, XACK is asserted by the slave before valid data is available or is accepted, in order to avoid unnecessary wait states with the common 16-bit microprocessors.

Compliance Notation:
Memory Module: Slave D16, M20

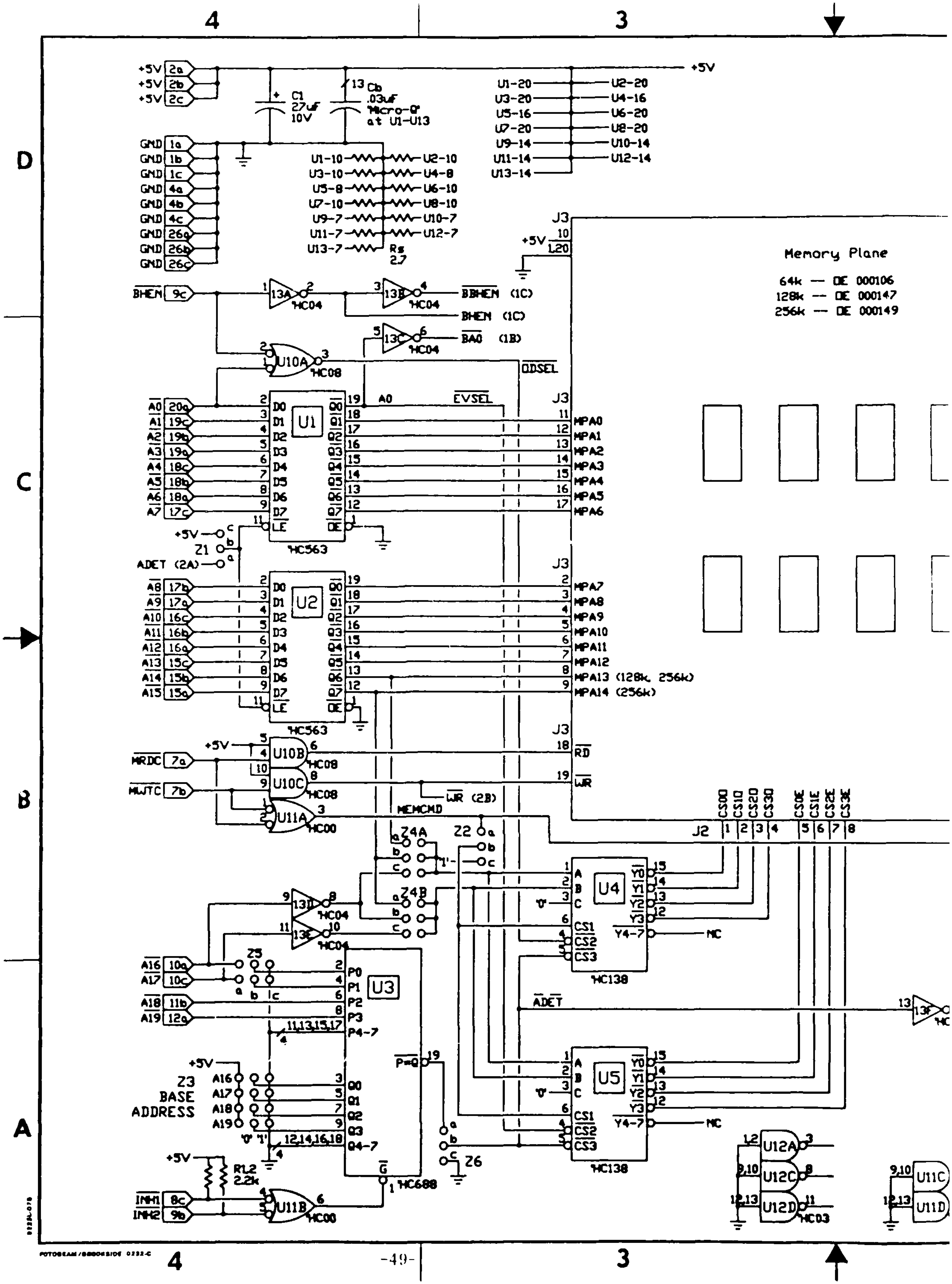
Circuit Description

The backplane address signals are buffered by U1 and U2, which drive the high capacitive load of the memory plane. Transparent latch devices perform the "address gate" function without the inefficiency inherent in a tristate driver/pullup implementation. The board base address is detected by comparator U3; decoders U4 and U5 generate the chip select signals to the memory devices in the Odd and Even halves of the Memory Plane.

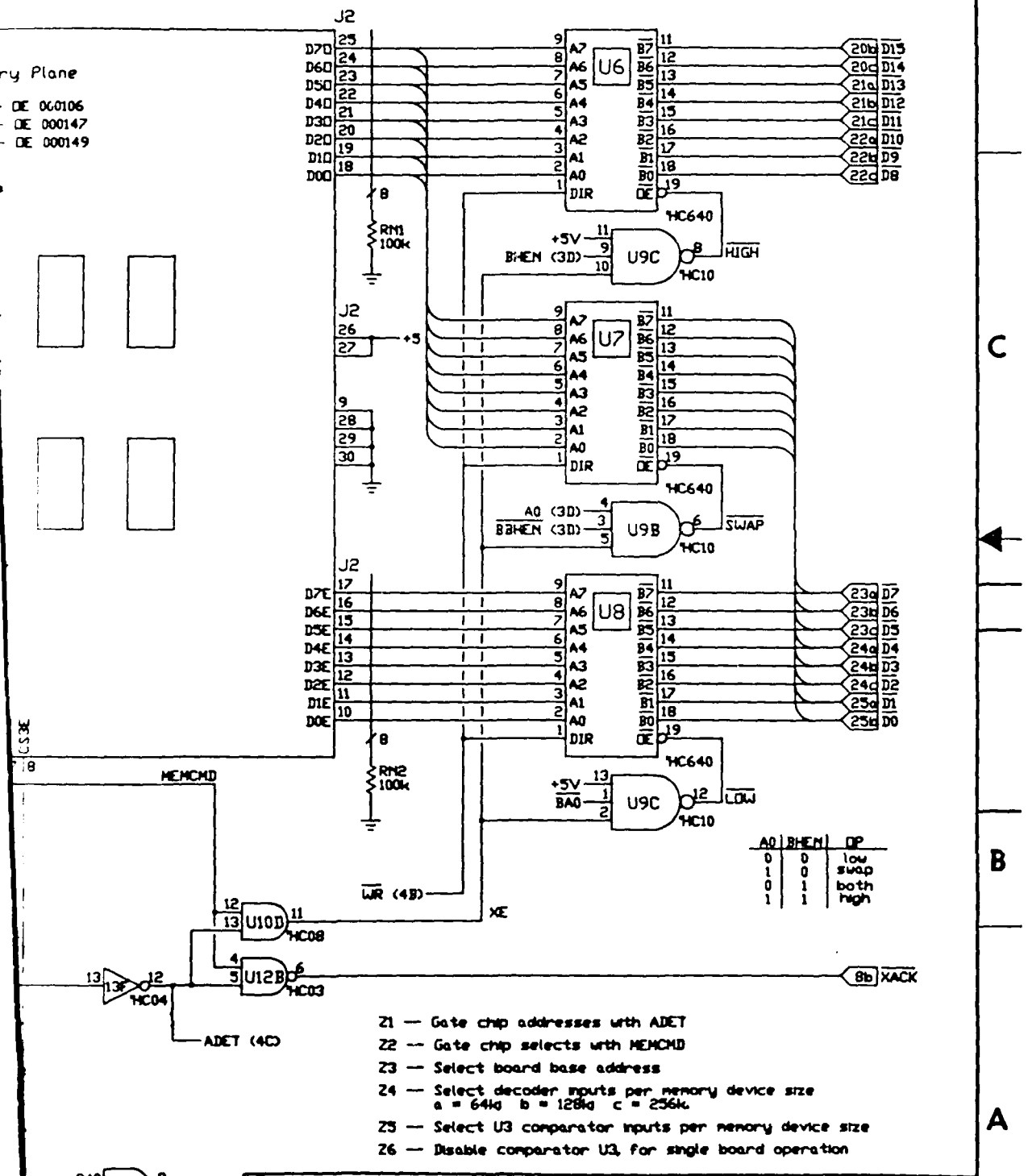
In accordance with IEEE-796, the memory module is organized as a linear sequence of byte locations. The bytes may be accessed one at a time, at alternating even and odd addresses, or two at a time (in words), at even addresses only. U9, U10, and U13 generate the signals which control data transfer, as specified by the following truth table:

A0	BHEN	EVSEL	ODSEL	Xcvr Enabled	Operation
0	0	1	0	low	even-address byte on D0-D7
1	0	0	1	swap	odd-address byte D0-D7
0	1	1	1	both	even-address word on D0-D15
1	1	-	-		not used

These conventions allow the Memory Module to be accessed by either 8- or 16-bit masters.


4
3
D
C
B
A
+5V 2a
+5V 2b
+5V 2c
GND 1a
GND 1b
GND 1c
GND 4a
GND 4b
GND 4c
GND 26a
GND 26b
GND 26c
C1 27uF 10V
13 Cb .03uF "Micro-Q" at U1-U13
U1-10 U2-10
U3-10 U4-8
U5-8 U6-10
U7-10 U8-10
U9-7 U10-7
U11-7 U12-7
U13-7
Rs 27
+5V
U1-20 U2-20
U3-20 U4-16
U5-16 U6-20
U7-20 U8-20
U9-14 U10-14
U11-14 U12-14
U13-14
J3
Memory Plane
64k — DE 000106
128k — DE 000147
256k — DE 000149
BHEN 9c
13A 'HC04
13B 'HC04
BBHEN (1C)
BHEN (1C)
13C 'HC04
BA0 (1B)
U10A 'HC08
ODSEL
EVSEL
A0
A0 20a
A1 19c
A2 19b
A3 19a
A4 18c
A5 18b
A6 18a
A7 17c
U1
'HC563
MPA0
MPA1
MPA2
MPA3
MPA4
MPA5
MPA6
Z1
ADET (2A)
A8 17b
A9 17a
A10 16c
A11 16b
A12 16a
A13 15c
A14 15b
A15 15a
U2
'HC563
MPA7
MPA8
MPA9
MPA10
MPA11
MPA12
MPA13 (128k, 256k)
MPA14 (256k)
MRDC 7a
MWTC 7b
U10B 'HC08
U10C 'HC08
RD
WR
WR (2B)
U11A 'HC00
MEMCMD
Z4A
Z2
Z4B
13D 'HC04
13E 'HC04
J2
CS0O CS1O CS2O CS3O
CS0E CS1E CS2E CS3E
U4
'HC138
NC
A16 10a
A17 10c
A18 11b
A19 12a
Z5
U3
'HC688
P=Q
ADET
13F
Z3 BASE ADDRESS
U5
'HC138
Z6
U12A
U12C
U12D 'HC03
U11C
U11D
+5V
RL2 2.2k
INH1 8c
INH2 9b
U11B 'HC00
FOTOBEAM / BROOKSIDE 0232-C

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		Add Z6	7/29/86	ccm



Z1 — Gate chip addresses with ADET
Z2 — Gate chip selects with MEMCMD
Z3 — Select board base address
Z4 — Select decoder inputs per memory device size
a = 64kg b = 128kg c = 256k
Z5 — Select U3 comparator inputs per memory device size
Z6 — Disable comparator U3, for single board operation

WOODS HOLE OCEANOGRAPHIC INSTITUTION ENGINEERING DEPT. WOODS HOLE, MA. 02543		TITLE INSTRUMENT BUS MEMORY CONTROL	
CONTRACT NO.	CODE NO		
BY MELLINGER	DATE 11/3/85	SIZE C	DWG. NO. 000128 — 1 OF 1 — REV

Instrument Bus
Memory Control
OE Dwg. 00128

Rev: none

Designation	Quan	Value	Rating	Type	Mfgr and Part Number
R1,2	2	2.2k	1/4W	5% Carbon Film	
Rs	13	2.7	1/8W	Carbon Comp	Allen-Bradley 'BB'
RN1,2	2	100k x 9		SIP Network	Dale MSP10A01-104G
C1	1	27uF	10V	Solid Tantalum	CSR13-M39003/01-2496 (Sprague)
Cb	5	20nF	14 pin	Micro-Q	Rogers uQ-14.02
Cb	2	30nF	16 pin	Micro-Q	Rogers uQ-16.03
Cb	6	30nF	20 pin	Micro-Q	Rogers uQ-20.03
U1,2	2	74HC563	Octal Inverting Latch		Mot. 74HC563J (DS)
U3	1	74HC688	Octal Comparator		Mot. 74HC688J (DS)
U4,5	2	74HC138	3-8 Decoder		Mot. 74HC138J (DS)
U6,7,8	3	74HC640	Octal Inverting Transceiver		Mot. 74HC640J (DS)
U9	1	74HC10	Triple NAND		Mot. 74HC10J (DS)
U10	1	74HC08	Quad AND		Mot. 74HC08J (DS)
U11	1	74HC00	Quad NAND		Mot. 74HC00J (DS)
U12	1	74HC03	Quad NAND OD		Mot. 74HC03J (DS)
U13	1	74HC04	Hex Inverter		Mot. 74HC04J (DS)
P1	1	DIN Connector STV-C 96-M-abc			ERNI 533-402
S2,3	30	Socket Strip (board interconnect)			Samtec SS-120-T-2
Z1-6	45	Shunt/Wrap Post			Samtec TSW-136-07-G-S
	11	Shunt			AMP 530153-2

4.2.5 64k Memory Plane

OE Dwg 00106
Revision: none Date: 27 August 1985 By: ecm

Description

The 64k Memory Plane contains 8 bytewide memory devices, either RAM or PROM. The board mounts on and works in conjunction with the Memory Control Board to form a 64k Memory Module.

Configuration

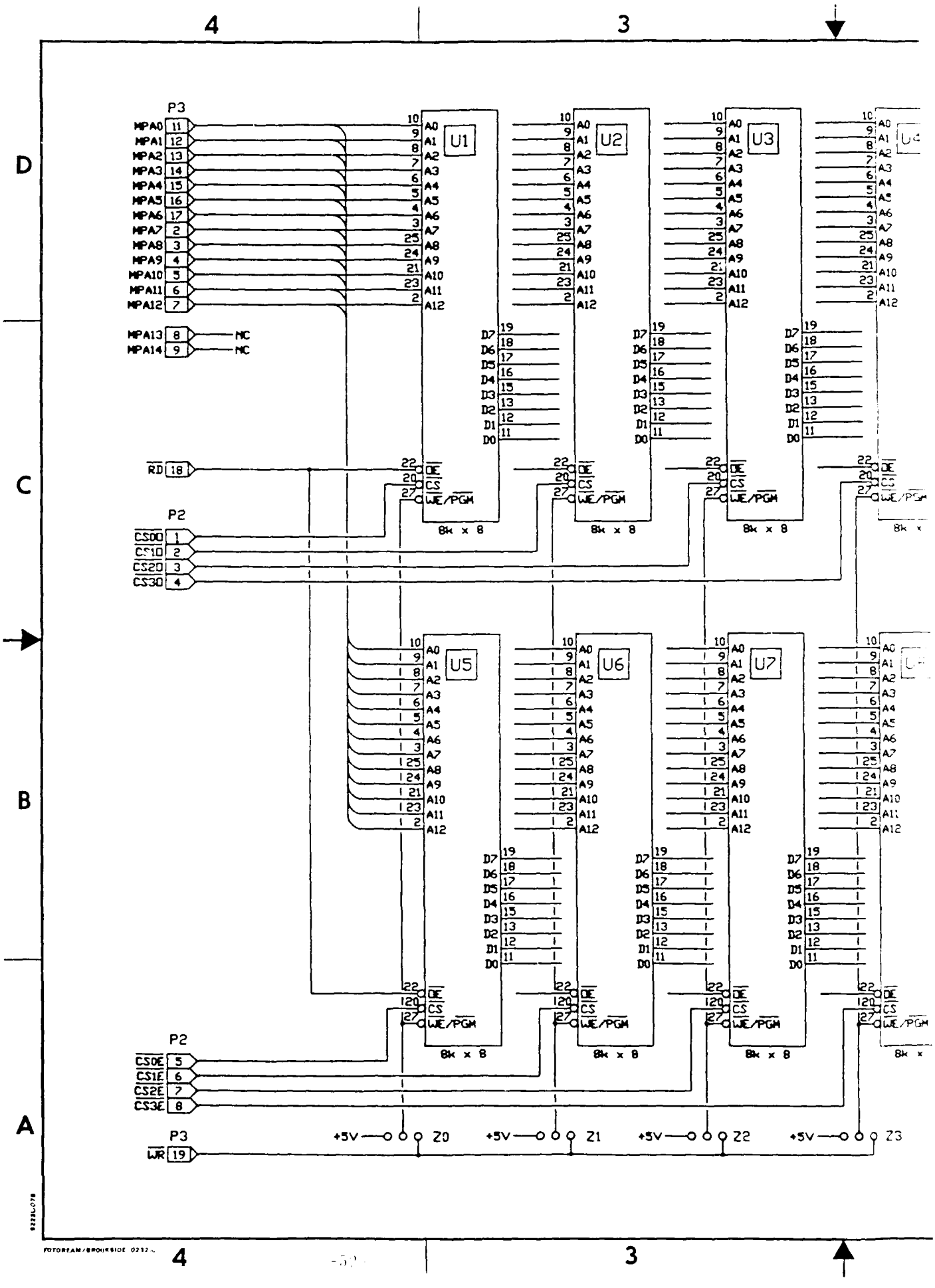
Required for operation: Z0-Z3
Optional: none

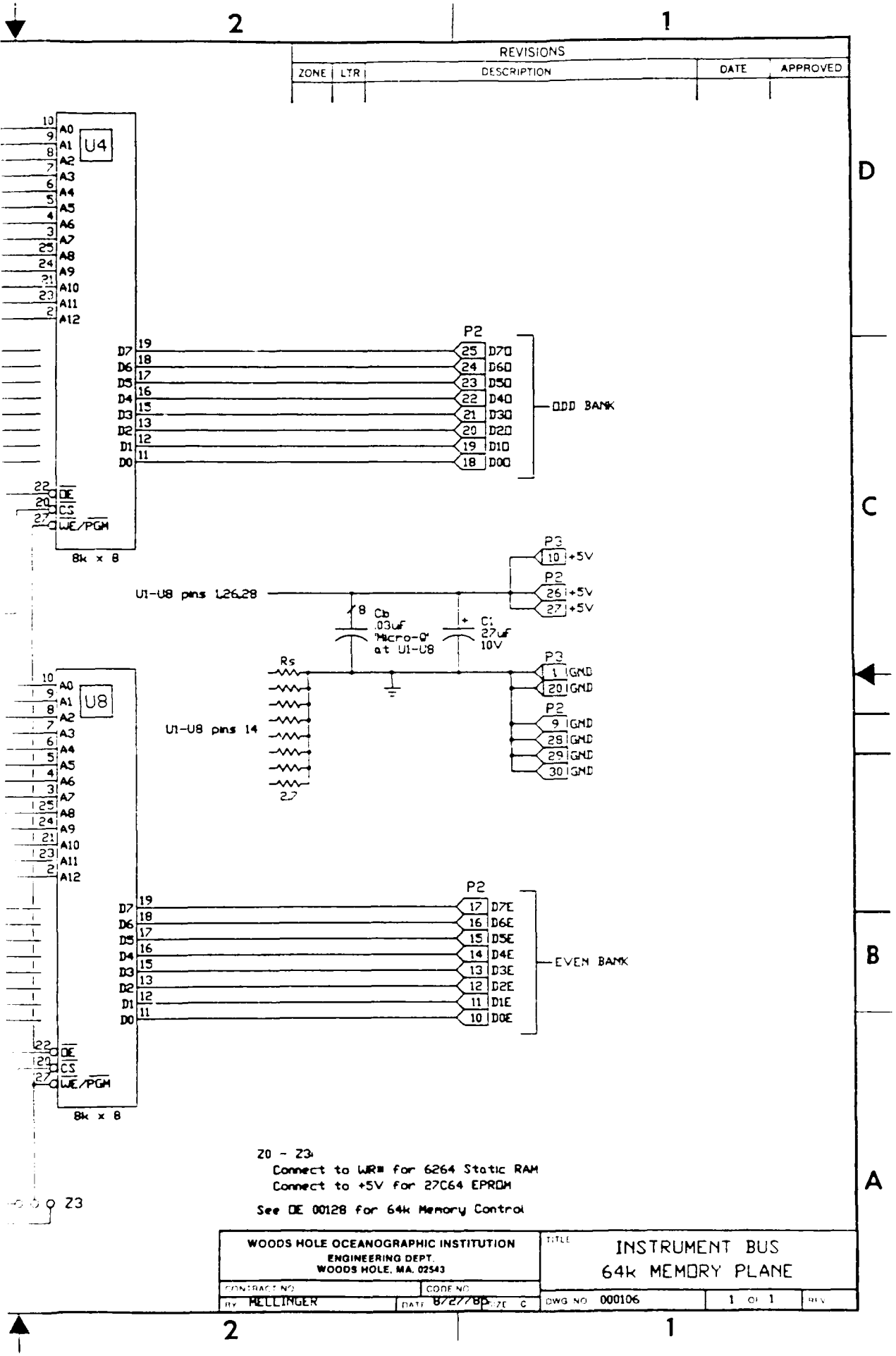
Z0-Z3: ROM/RAM Select

Each of the 8 memory sites on the Memory Plane can be occupied by either ROM (EPROM, EEPROM, PROM, etc.) or RAM devices. The RAMs require WR* on pin 27; the PROMs require pin 27 to be connected to +5V. Since the memory sites are interleaved on an odd/even basis, there are effectively four 16k blocks that can be independently selected for RAM or ROM. Shunt plugs are required at Z0-Z3 to perform this function.

Circuit Description

The 64k Memory Plane contains only memory devices. The eight devices are organized into two banks, the odd bank consisting of U1-U4 and the even bank of U5-U8. Address, Read/Write, and Chip Select signals are all generated on the companion Memory Control board.


4
3
D
C
B
A
P3
MPA0 11
MPA1 12
MPA2 13
MPA3 14
MPA4 15
MPA5 16
MPA6 17
MPA7 2
MPA8 3
MPA9 4
MPA10 5
MPA11 6
MPA12 7
MPA13 8
MPA14 9
NC
NC
RD 18
P2
CS0D 1
CS1D 2
CS2D 3
CS3D 4
U1
U2
U3
U4
U5
U6
U7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
D7 D6 D5 D4 D3 D2 D1 D0
OE CS WE/PGM
8k x 8
P2
CS0E 5
CS1E 6
CS2E 7
CS3E 8
P3
WR 19
+5V Z0
+5V Z1
+5V Z2
+5V Z3


2
1
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
D
C
B
A
U4
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
D7
D6
D5
D4
D3
D2
D1
D0
P2
25 D7O
24 D6O
23 D5O
22 D4O
21 D3O
20 D2O
19 D1O
18 D0O
ODD BANK
OE
CS
WE/PGM
8k x 8
P3
10 +5V
P2
26 +5V
27 +5V
U1-U8 pins 1,26,28
8 Cb
.03uF
"Micro-Q"
at U1-U8
C1
27uF
10V
Rs
2.7
U1-U8 pins 14
P3
1 GND
20 GND
P2
9 GND
28 GND
29 GND
30 GND
U8
P2
17 D7E
16 D6E
15 D5E
14 D4E
13 D3E
12 D2E
11 D1E
10 D0E
EVEN BANK
Z0 - Z3
Connect to WR# for 6264 Static RAM
Connect to +5V for 27C64 EPROM
See DE 00128 for 64k Memory Control
Z3
WOODS HOLE OCEANOGRAPHIC INSTITUTION
ENGINEERING DEPT.
WOODS HOLE, MA. 02543
TITLE
INSTRUMENT BUS
64k MEMORY PLANE
CONTRACT NO
CODE NO
BY MELLINGER
DATE 8/27/86
SIZE C
DWG NO 000106
1 OF 1
REV

Instrument Pus
64k Memory Plane
OE Dwg. 00106

Rev: none

Designation	Quan	Value	Rating	Type	Mfgr and Part Number
Rs	8	2.7	1/8W	Carbon Comp	Allen-Bradley 'BB'
C1	1	27uF	10V	Solid Tantalum	CSR13-M39003/01-2496 (Sprague)
Cb	8	30nF	28 pin	Micro-Q	Rogers uQ-28.03
U1-8	8	8k x 8	200 nsec	Bytewide Memory	27C64 (Hitachi 27C64G-20) or 6264 (NEC D4464C-20L)
		28 pin	.120" hgt.	Low Profile Socket	Samtec ICO-628-L-GT
P1	0	(not used)			
P2,3	50	Interconnect Strip			Samtec BBL-120-G-F
J0-3	12	Shunt/Wrap Post			Samtec TSW-136-07-G-S
	4	Shunt			AMP 530153-2

4.2.6 Dual Serial I/O

OE Dwg 00101
Rev: C Date: 15 May 1986 By: ecm

Description

The Dual Serial board provides two Harris 82C52 serial asynchronous I/O ports, each with with on-chip oscillator and baud rate generator. A separate 4060B oscillator circuit is also available for low frequency (38.4 kHz - 307.2 kHz) clock generation, allowing low power standby in power critical applications. Onboard level shifters interface the UART CMOS logic levels to SAIL 20 mA current loop and SAIL Open Collector formats. The SAIL signals are available on a separate 8-pin connector at the top of the board, as well as on four of the unused backplane pins. A 20-pin expansion connector makes the UART CMOS I/O and handshaking signals available to an auxiliary "level shifter" board, normally located adjacent to the Dual Serial board in the card rack, which can be used to provide other communication formats if required. Examples of these would include RS-232, RS-485, SAIL/FSK, or fiber optic formats.

Configuration

Required for operation: Z1,3,4
Optional: Z2,5

Z1: Base Address

The Dual Serial board occupies 8 locations in the IEEE-796 I/O address space. Z1 selects the base address in this space. All 5 shunt plugs must be installed for correct operation. The 8 locations have the following assignments:

Base+0	Uart 1 (U7) Data
Base+1	Uart 1 (U7) Control
Base+2	Uart 1 (U7) Modem Control
Base+3	Uart 1 (U7) Baud Rate select
Base+4	Uart 2 (U6) Data
Base+5	Uart 2 (U6) Control
Base+6	Uart 2 (U6) Modem Control
Base+7	Uart 2 (U6) Baud Rate select

Z2: Interrupt Select

The Dual Serial board has five available interrupt sources: the INTR and Data Ready outputs from each UART, and RFAP from the SAIL current loop adapter. After conditioning by pull-up resistors these five source signals are available on the input side of Z2. Wire wrap jumpers are used to link selected interrupt sources to interrupt lines INT0* - INT7* on the backplane.

Z3: UART 2 Clock Source Select

Three separate Baud Rate Clock sources are available to UART 2 (U6): the on-chip crystal oscillator, the external (U11) oscillator, or the backplane CCLK* signal. The Z3 shunt, which must be present for operation, selects between a local oscillator (when shunting pins 1 and 2) and the CCLK* signal (when shunting pins 2 and 3). Choice of local oscillator is by selective component installation; crystal frequency will normally be a baud-rate multiple between 153.6 kHz and 1.2288 MHz. To use the U6 UART oscillator, install crystal X1 and load capacitors C4 and C5. Note that U6 has a lower crystal frequency limit of 1 Mhz, and has experienced noise problems in the past (see Application Notes below). To use the U11 4060B oscillator, install U11, crystal X2, and associated components R4, R5, C6, and C7. U11 is the recommended oscillator for baud rates of 9600 or less, due to its low power consumption (about 1 mA/MHz) and noise free operation.

Z4: UART 1 Clock Source Select

Two Baud Rate Clock sources are available to UART 1 (U7): The Clock Output signal from UART 2 (U6), or the backplane CCLK* signal. The Z4 shunt, which must be present for operation, selects between backplane CCLK* (when shunting pins 1 and 2), and U6 Clock Out (when shunting pins 2 and 3). Note that U6 must be installed and its Baud Rate Select Register (Base+3) programmed for the correct Clock Out frequency when the second option is used.

Z5: SAIL Level Shifter Select

Using Z5, either of the two UARTs can be connected to either of the two SAIL level shifter circuits (Current Loop or Open Collector) on the Dual Serial board. A typical configuration, using UART 2 (U6) for Current Loop and UART 1 (U7) for Open Collector, would be configured as follows:

Z5 Column 1: Shunt Row A and B (U7 out to Q1 in)
Z5 Column 2: Shunt Row B and C (U6 out to U10 in)
Z5 Column 3: Shunt Row A and B (Q1 out to U7 in)
Z5 Column 4: Shunt Row B and C (U10 out to U6 in)

Note that when an auxiliary level shifter board is employed and P2 is in use, the columns of Z5 corresponding to the UART in use (columns 2 and 4 for U6, and 1 and 3 for U7) must be left open.

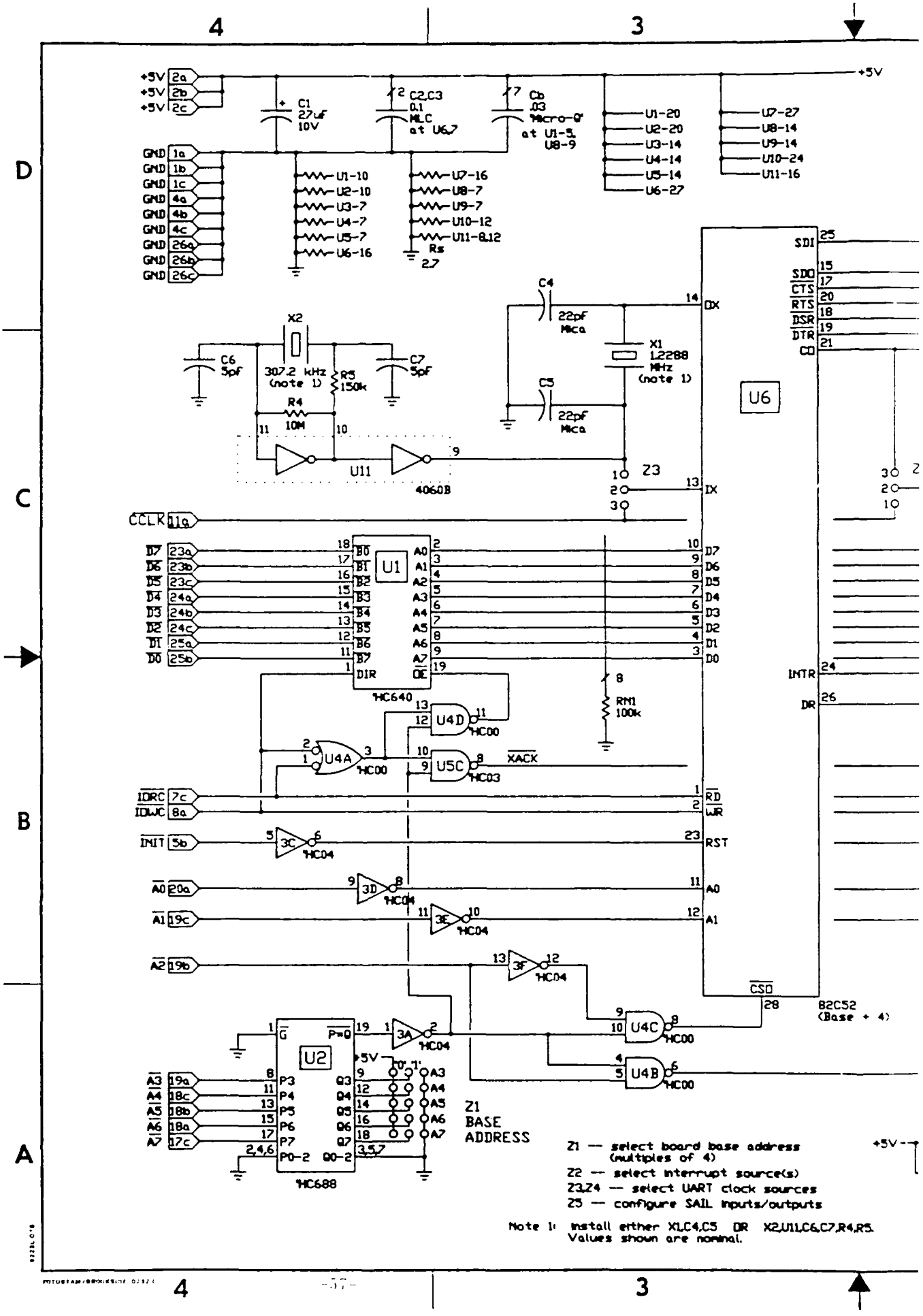
Application Notes

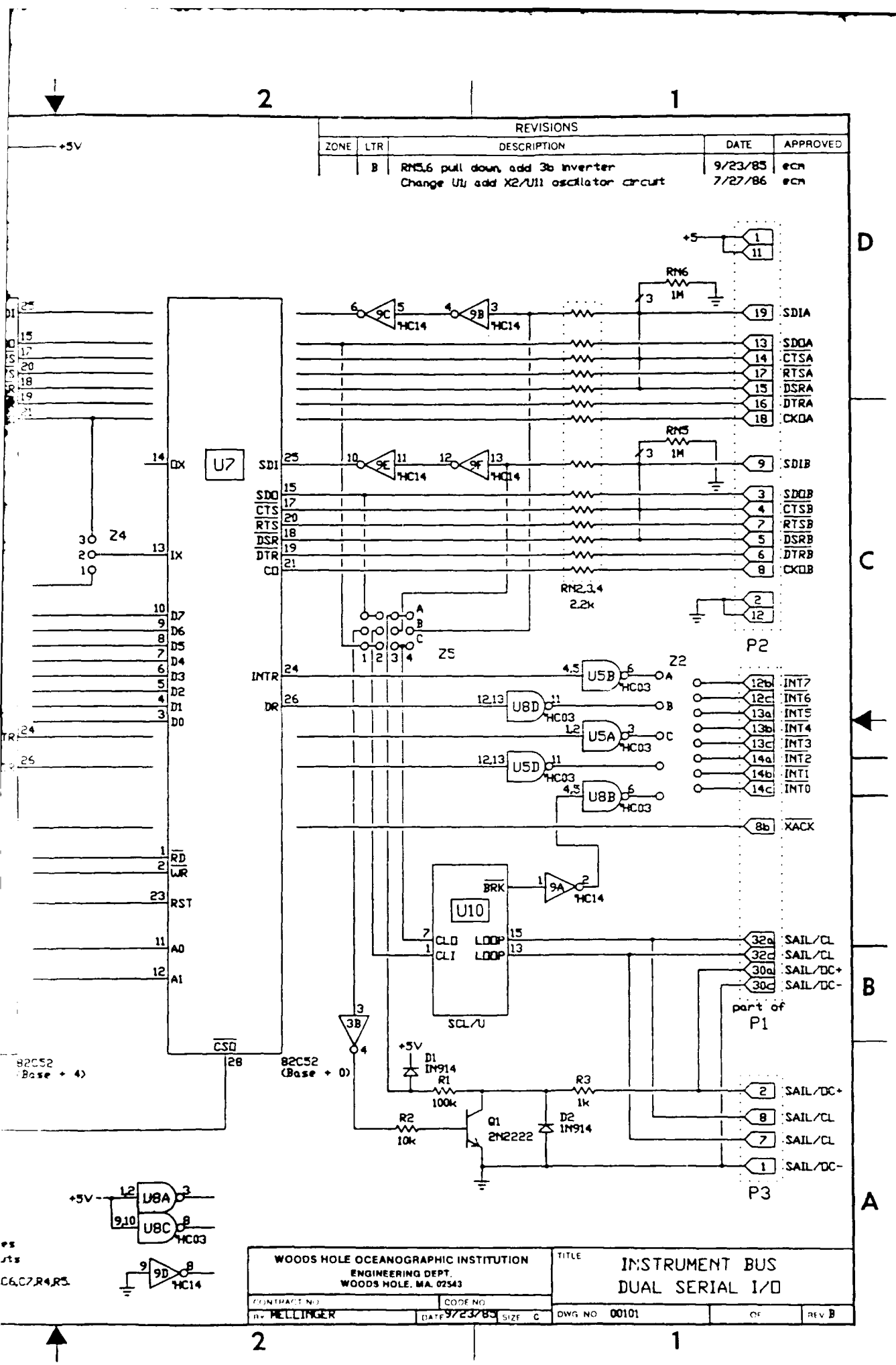
In the past, noise coupling problems have been observed between U6 pins 12 (address 1) and 13 (oscillator input) due to high inter-pin capacitance within the 82C52. The problem appears as incorrect (high) U6 baud rate and is more severe at low temperatures. Use of the U11 oscillator avoids this problem but limits operation to 19.2 kBaud. It is not known if Harris admits to or intends to fix this 82C52 problem in the future.

Circuit Description

Circuitry on the Dual Serial board is straightforward. U1-5 form the standard IEEE-796 I/O interface. U6 and U7 are the UARTs, with Schmitt

triggers from U9 added at the serial inputs for increased noise immunity. U10 is the CMOS-to-20mA level shifter, with U9 providing hysteresis on the BREAK output. Q1 is the Open Collector driver. R3, D1, and D2 provide overload protection, while R1 prevents loading the OC SAIL bus in the event of power failure at the Dual Serial board.


4
3
D
C
B
A
+5V
GND
C1 27uF 10V
C2,C3 0.1 MLC at U6,7
C6 5pf
C7 5pf
X2 307.2 kHz (note 1)
R5 150k
R4 10M
U11 4060B
C4 22pf Mica
C5 22pf Mica
X1 1.2288 MHz (note 1)
U6
U1
HC640
U4A
U4B
U4C
U4D
U5C
3A
3C
3D
3E
3F
U2
HC688
RN1 100k
XACK
RST
RD
WR
CSO
82C52 (Base + 4)
Z1 BASE ADDRESS
Z1 — select board base address (multiples of 4)
Z2 — select interrupt source(s)
Z3,Z4 — select UART clock sources
Z5 — configure SAIL inputs/outputs
Note 1: Install either X1,C4,C5 OR X2,U11,C6,C7,R4,R5. Values shown are nominal.


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B | RN5,6 pull down, add 3b inverter | 9/23/85 | ecm
Change U1, add X2/U11 oscillator circuit | 7/27/86 | ecm
+5V
U7
U10
U5B
U8D
U5A
U5D
U8B
U8A
U8C
9C
9B
9E
9F
9A
9D
3B
HC14
HC03
RN6
RN5
1M
RN2,3,4
2.2k
Z4
Z5
Z2
P2
P1
P3
SDIA
SDOA
CTSA
RTSA
DSRA
DTRA
CKOA
SDIB
SDOB
CTSB
RTSB
DSRB
DTRB
CKOB
INT7
INT6
INT5
INT4
INT3
INT2
INT1
INT0
XACK
SAIL/CL
SAIL/DC+
SAIL/DC-
part of
SCL/U
BRK
CLO
CLI
LOOP
D1
IN914
R1
100k
R2
10k
R3
1k
Q1
2N2222
D2
IN914
82C52
(Base + 4)
82C52
(Base + 0)
WOODS HOLE OCEANOGRAPHIC INSTITUTION
ENGINEERING DEPT.
WOODS HOLE, MA. 02543
TITLE
INSTRUMENT BUS
DUAL SERIAL I/O
BY MELLINGER
DATE 9/23/85
SIZE C
DWG NO 00101
REV B

Instrument Bus
Dual Serial I/O
CE Dwg. 00101

Rev B 15 May 1986 ecm

Designation	Quan	Value	Rating	Type	Rev	Mfgr and Part Number
R1	1	100k	1/4W	5% Carbon Film	B	
R2	1	10k	1/4W	5% Carbon Film		
R3	1	1k	1/4W	5% Carbon Film		
R4	1	10M	1/4W	5% Carbon Film	C	
R5	1	150k	1/4W	5% Carbon Film	C	
Rs	11	2.7	1/8W	Carbon Comp		Allen-Bradley 'BB'
RN1	1	100k x 9		SIP Network		Dale MSP10A01-104G
RN2,3,4	3	4.7k x 5	isolated	SIP Network		Dale MSP10A03-472G
RN5,6	2	1M x 3		SIP Network		Dale CSC04A01-105G
C1	1	27uF	10V	Solid Tantalum		CSR13-M39003/01-2496 (Sprague)
C2,3	2	100nF	50V	CK06 Ceramic		
C4,5	2	22pF		Silver Mica		
C6,7	2	5pF		Silver Mica	C	
Cb	5	20nF	14 pin	Micro-Q		Rogers uQ-14.02
Cb	1	30nF	16 pin	Micro-Q		Rogers uQ-16.03
Cb	2	30nF	20 pin	Micro-Q		Rogers uQ-20.03
D1,2	2	1N914				
Q1	1	2N2222A				
X1	1	as req'd	AT cut			see 82C52 spec sheet
X2	1	as req'd	tuning fork		C	Statek CX-1V (if X1 not used)
U1	1	74HC640	Octal Inverting Transceiver			Mot. 74HC640J (DS)
U2	1	74HC688	Octal Comparator			Mot. 74HC688J (DS)
U3	1	74HC04	Hex Inverter			Mot. 74HC04J (DS)
U4	1	74HC00	Quad NAND			Mot. 74HC00J (DS)
U5,8	2	74HC03	Quad NAND OD			Mot. 74HC03J (DS)
U6,7	2	82C52	UART/BRG			Harris ID-82C52
U9	1	74HC14	Hex Schmitt			Mot 74HC14J (DS)
U10	1	SCL/U	20mA/CMOS Converter			WET SCL/U
U11	1	4060B	Oscillator/Divider		C	RCA CD4060BF (XV)
P1	1	DIN Connector	STV-C 96-M-abc			ERNI 533-402
P2	1	AmpLatch 20				AMP 102326-4
P3	1	AmpModU 8				AMP 87578-1
Z1-5	46	Shunt/Wrap Post				Samtec TSW-136-07-G-S
	11	Shunt				AMP 530153-2

4.2.7 Parallel I/O

OE Dwg 00102
Rev: none Date: 29 July 1986 By: ecm

Description

The Parallel I/O board provides a single Harris 82C55A Programmable Peripheral Interface port. This device, depending upon the mode programmed, provides three basic 8-bit parallel input/output ports, or two ports with assorted handshaking options. No level shifting capability is provided on the board; however unused board area (approximately 6 sq. in.) is hole-gridded to allow custom level shifter circuits to be wire-wrapped as required. A 40-pin AmpLatch (ribbon cable) connector is available at the top of the board for large-signal-count applications, in addition to an 8-pin AmpModU connector for discrete-wired I/O.

Configuration

Required for operation: Z1
Optional: Z2

Z1: Base Address

The Parallel I/O board occupies 4 locations in the IEEE-796 I/O address space. Z1 selects the board base address in this space. All 6 shunt plugs must be installed for correct operation. The 4 locations have the following assignments:

Base + 0	Port A Data
Base + 1	Port B Data
Base + 2	Port C Data
Base + 3	Mode Control

Z2: Interrupt Select

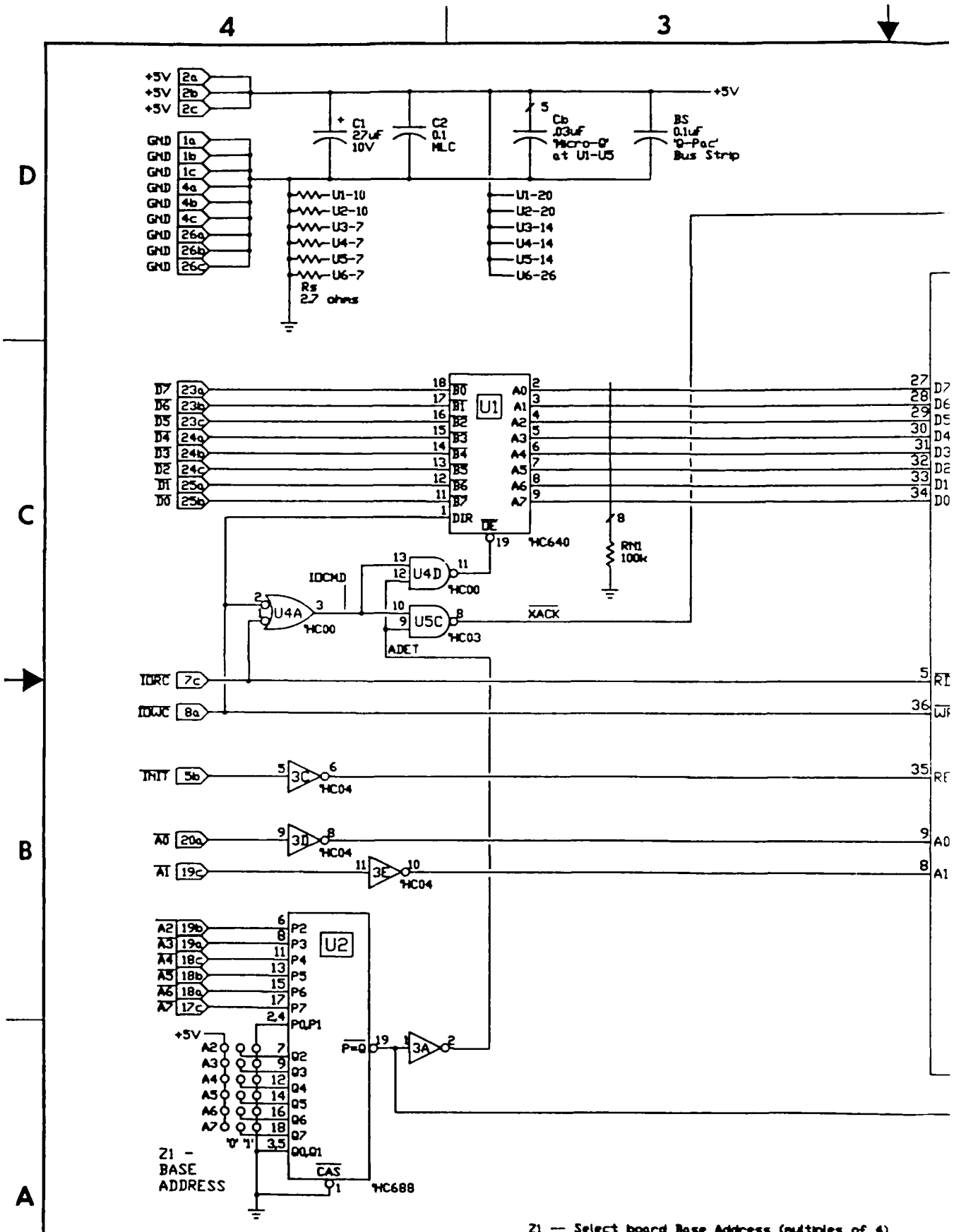
The Parallel I/O board has two interrupt sources, available from the 82C55A during certain handshaking modes. These are conditioned by Open Drain gates and made available on the input side of Z2. Wire-wrap jumpers are used to link selected interrupt sources to interrupt request lines INT0* - INT7* on the backplane.

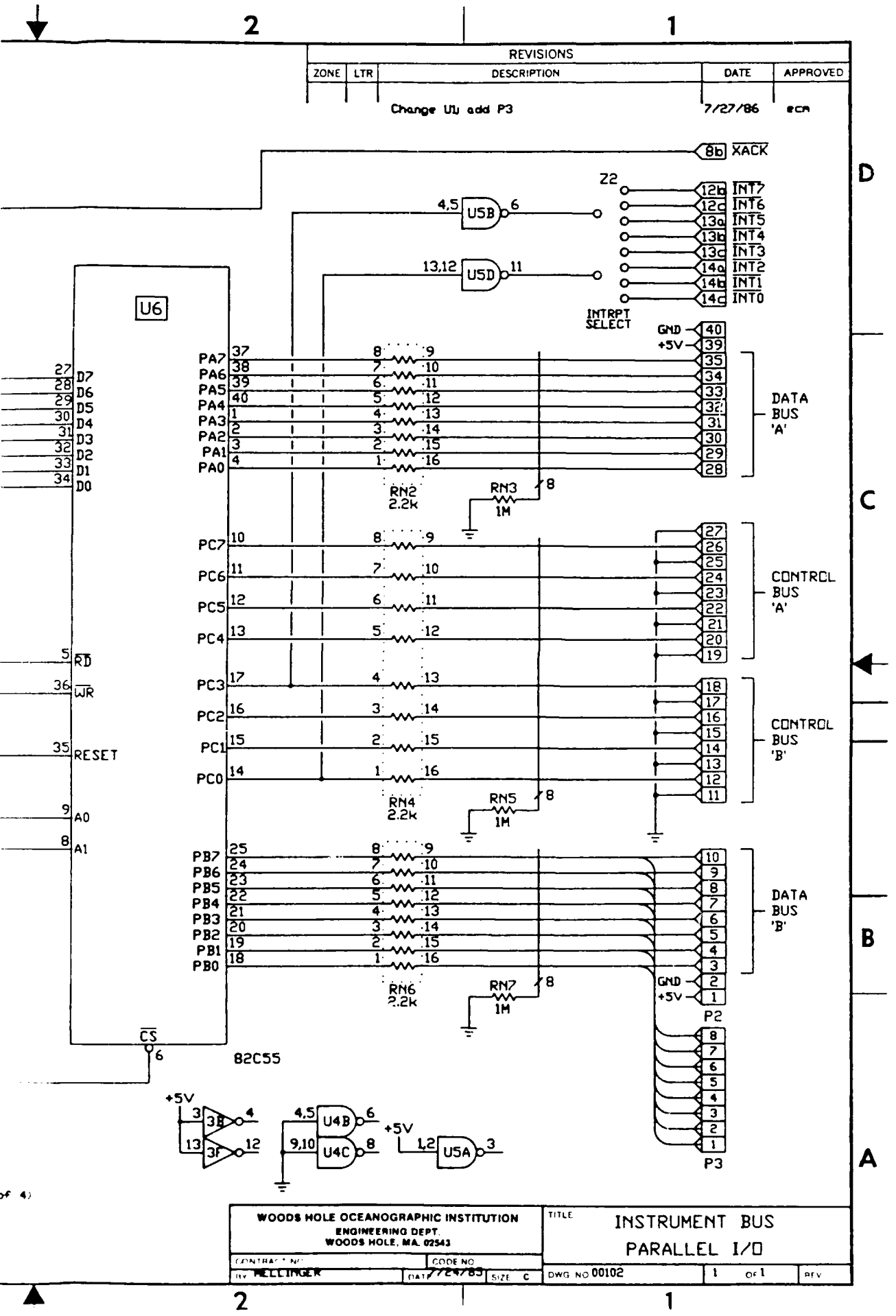
Application Notes

The values given for resistor networks RN2 through RN7 are nominal and may be changed as required by applications. Harris 82C55A devices contain internal input pull-up circuits, hence RN 3,5, and 7 may not be required when those devices are used. For access to auxiliary level shifters, omit RN2,4,6 and install wire-wrap sockets at those locations. Wire-wrap from the sockets' input (U6) side to the level shifters, then back to the sockets' output (P2 or P3) side.

Circuit Description

The Parallel I/O board has a minimum of extra circuitry. U1 through U5 form the standard IEEE-796 I/O interface with XACK* handshake. U6 is the I/O port chip. Resistor networks RN2,4,6 provide a degree of transient immunity and latch-up protection by limiting fault current in to or out of U6, while RN3,5,7 prevent floating CMOS inputs. The control strobe signals from U6 Port C passing through ribbon cable connector P2 are interleaved with grounds to reduce capacitive coupling on long cable runs.


4
3
D
C
B
A
+5V 2a
+5V 2b
+5V 2c
GND 1a
GND 1b
GND 1c
GND 4a
GND 4b
GND 4c
GND 26a
GND 26b
GND 26c
C1 27uF 10V
C2 0.1 MLC
5
Cb .03uF Micro-D at U1-U5
BS 0.1uF D-Pac Bus Strip
+5V
U1-10
U2-10
U3-7
U4-7
U5-7
U6-7
Rs 2.7 ohms
U1-20
U2-20
U3-14
U4-14
U5-14
U6-26
D7 23a
D6 23b
D5 23c
D4 24a
D3 24b
D2 24c
D1 25a
D0 25b
U1
DIR
DE
74HC640
RN1 100k
IOCMD
U4A
U4D
U5C
74HC00
74HC03
XACK
ADET
IORC 7c
IOWC 8a
INIT 5b
74HC04
A0 20a
A1 19c
U2
A2 19b
A3 19a
A4 18c
A5 18b
A6 18a
A7 17c
P0,P1
P=Q
74HC688
Z1 - BASE ADDRESS
Z1 -- Select board Base Address (multiples of 4)
Z2 -- Select Interrupt Request


2
1
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
Change U1J add P3 | 7/27/86 | ecm
8b XACK
Z2
12b INT7
12c INT6
13a INT5
13b INT4
13c INT3
14a INT2
14b INT1
14c INT0
4,5 U5B 6
13,12 U5D 11
INTRPT SELECT
U6
GND 40
+5V 39
PA7 37
PA6 38
PA5 39
PA4 40
PA3 1
PA2 2
PA1 3
PA0 4
RN2 2.2k
RN3 1M
DATA BUS 'A'
27 D7
28 D6
29 D5
30 D4
31 D3
32 D2
33 D1
34 D0
PC7 10
PC6 11
PC5 12
PC4 13
PC3 17
PC2 16
PC1 15
PC0 14
RN4 2.2k
RN5 1M
CONTROL BUS 'A'
CONTROL BUS 'B'
5 RD
36 WR
35 RESET
9 A0
8 A1
PB7 25
PB6 24
PB5 23
PB4 22
PB3 21
PB2 20
PB1 19
PB0 18
RN6 2.2k
RN7 1M
DATA BUS 'B'
GND 2
+5V 1
P2
P3
CS 6
82C55
+5V
3 3E 4
13 3F 12
4,5 U4B 6
9,10 U4C 8
+5V
1,2 U5A 3
D
C
B
A
WOODS HOLE OCEANOGRAPHIC INSTITUTION
ENGINEERING DEPT.
WOODS HOLE, MA. 02543
TITLE
INSTRUMENT BUS
PARALLEL I/O
CONTRACT NO
CODE NO
BY MELLINGER
DATE 7/24/85
SIZE C
DWG NO 00102
1 OF 1
REV

Instrument Bus
Parallel I/O
OE Dwg. 00102

Rev: none Date: 21 March 1985 By: ecm

Designation	Quan	Value	Rating	Type	Rev	Mfgr and Part Number
RN1	1	100k x 9		SIP Network		Dale MSP10A01-104G
RN3,5,7	3	1M x 9		SIP Network		Dale MSP10A01-105G
RN2,4,6	3	2.2k x 8		DIP Network		Dale MDP1603-222G
Rs	6	2.7	1/8W	Carbon Comp		Allen-Bradley 'BB'
C1	1	27uF	10V	Solid Tantalum		CSR13-M39003/01-2496 (Sprague)
C2	1	100nF	50V	CK06 Ceramic		
Cb	3	20nF	14 pin	Micro-Q		Rogers uQ-14.02
Cb	2	30nF	20 pin	Micro-Q		Rogers uQ-20.03
BS	1	.1uF		Bus Strip		Rogers QV2-9.5.1(.1)
U1	1	74HC640	Octal Inverting Transceiver			Mot. 74HC640J (DS)
U2	1	74HC688	Octal Comparator			Mot. 74HC688J (DS)
U3	1	74HC04	Hex Inverter			Mot. 74HC04J (DS)
U4	1	74HC00	Quad NAND			Mot. 74HC00J (DS)
U5	1	74HC03	Quad NAND OD			Mot. 74HC03J (DS)
U6	1	82C55	Parallel I/O Port			Harris ID-82C55
P1	1	DIN Connector STV-C 96-M-abc				ERNI 533-402
P2	1	AmpLatch 40				AMP 102326-9
P3	1	AmpModU 8				AMP 87578-1
Z1,2	28	Shunt/Wrap Post				Samtec TSW-136-07-G-S
	3	Shunt				AMP 530153-2

4.2.8 Clock/Timebase

OE Dwg 00103
Rev: B Date: 27 July 1986 By: ecm

Description

The Clock/Timebase board provides a basic time and frequency standard capability for the Instrument Bus. The timebase and/or frequency standard is supplied by an onboard Temperature Compensated Crystal Oscillator (TCXO), whose frequency and temperature characteristics can be specified to match the application. A dedicated onboard regulator isolates the TCXO from drift and noise in the system +12V supply. The TCXO output is available through an 8-pin connector at the top of the board, and can optionally be prescaled by a binary ripple counter in ratios of up to 256. The timekeeping function is provided by a National 58167 Real-Time-Clock (RTC) chip, which can either operate from its own 32.768 kHz tuning-fork crystal oscillator, or be driven by an appropriately prescaled output from the TCXO. With the on-chip oscillator the clock will operate for roughly 18 hours without external +5V power, using a 0.22 Farad double-layer capacitor as a backup energy source.

Configuration

Required for operation: Z1,Z2,Z3
Optional: Z4,Z5

Z1: Base Address

The Clock/Timebase board occupies 32 locations in the IEEE-796 address space. Z1 selects the board base address in this space. All three shunt plugs must be installed for correct operation. The 32 locations have the following assignments:

Base + 0	RTC counter -- milliseconds
Base + 1	RTC counter -- tenths and hundredths
Base + 2	RTC counter -- seconds
Base + 3	RTC counter -- minutes
Base + 4	RTC counter -- hours
Base + 5	RTC counter -- day of week
Base + 6	RTC counter -- day of month
Base + 7	RTC counter -- month
Base + 8	RTC RAM -- milliseconds
Base + 9	RTC RAM -- tenths and hundredths
Base + 10	RTC RAM -- seconds
Base + 11	RTC RAM -- minutes
Base + 12	RTC RAM -- hours
Base + 13	RTC RAM -- day of week
Base + 14	RTC RAM -- day of month
Base + 15	RTC RAM -- month
Base + 16	RTC interrupt status register
Base + 17	RTC interrupt control register
Base + 18	RTC counter reset
Base + 19	RTC RAM reset

Base + 20	RTC rollover status bit
Base + 21	RTC 'GO' command
Base + 22	RTC Standby Interrupt*
Base + 23	not used
Base + 24	not used
Base + 25	not used
Base + 26	not used
Base + 27	not used
Base + 28	not used
Base + 29	not used
Base + 30	not used
Base + 31	test mode

Z2: Interrupt Select

The Clock/Timebase board has one interrupt source: the INTR output of the RTC chip. This output can be programmed for a periodic interrupt, or for "alarm clock" mode upon a match between RTC clock and RTC RAM. Wire-wrap jumpers at Z2 allow this signal to be connected to any desired interrupt request line on the backplane.

Z3: Wait State Select

The 58167A RTC chip has a specified address-to-command delay requirement of 100 nsec minimum, and a specified address-to-data access time of 1050 nsec (i.e. 1.05 usec). These specifications are typical for 1984-era RTC chips. Z3 is used to configure U6, the waitstate counter, to generate these delay times. Z3 CMD DELAY sets the number of CCLK cycles by which the bus Read (IORC) and Write (IOWC) commands are delayed before being applied to the RTC chip. Z3 ACCESS DELAY sets the number of CCLK cycles from IORC or IOWC active to XACK active, which forces the bus processor to wait until the RTC has output or input valid data before terminating the I/O operation.

One jumper must be installed in each half of Z3 for proper board operation. Z3 CMD DELAY should be set to provide a delay of at least 100 nsec with the CCLK in use in the system. Z3 ACCESS DELAY should be set for a total delay of at least 1050 nsec. In no case should CMD DELAY exceed ACCESS DELAY.

Z4: Timebase Source

This wire-wrap jumper allows either the onboard TCXO or the backplane CCLK signal to drive either divider U9 or jumper Z5.

Z5: Timebase Use

This wire-wrap jumper allows the timebase signals selected by Z4 to be routed either off the board via P1 and P2, or used to synchronize the RTC oscillator. For RTC synchonization a 50% duty cycle square wave at 32.768 kHz is required, either from the U9 divider or externally. This signal overdrives the RTC crystal oscillator through C4, which allows the RTC to continue oscillation with its own crystal in the event of external signal loss.

Application Notes

R6 is provided to pull the RTC chip PWR.DN* line low when the Clock/Timebase board is removed from the backplane. With the board in the rack and power off, the backplane INIT* signal must be pulled within a few tenths of a volt of ground to achieve low standby current in the RTC.

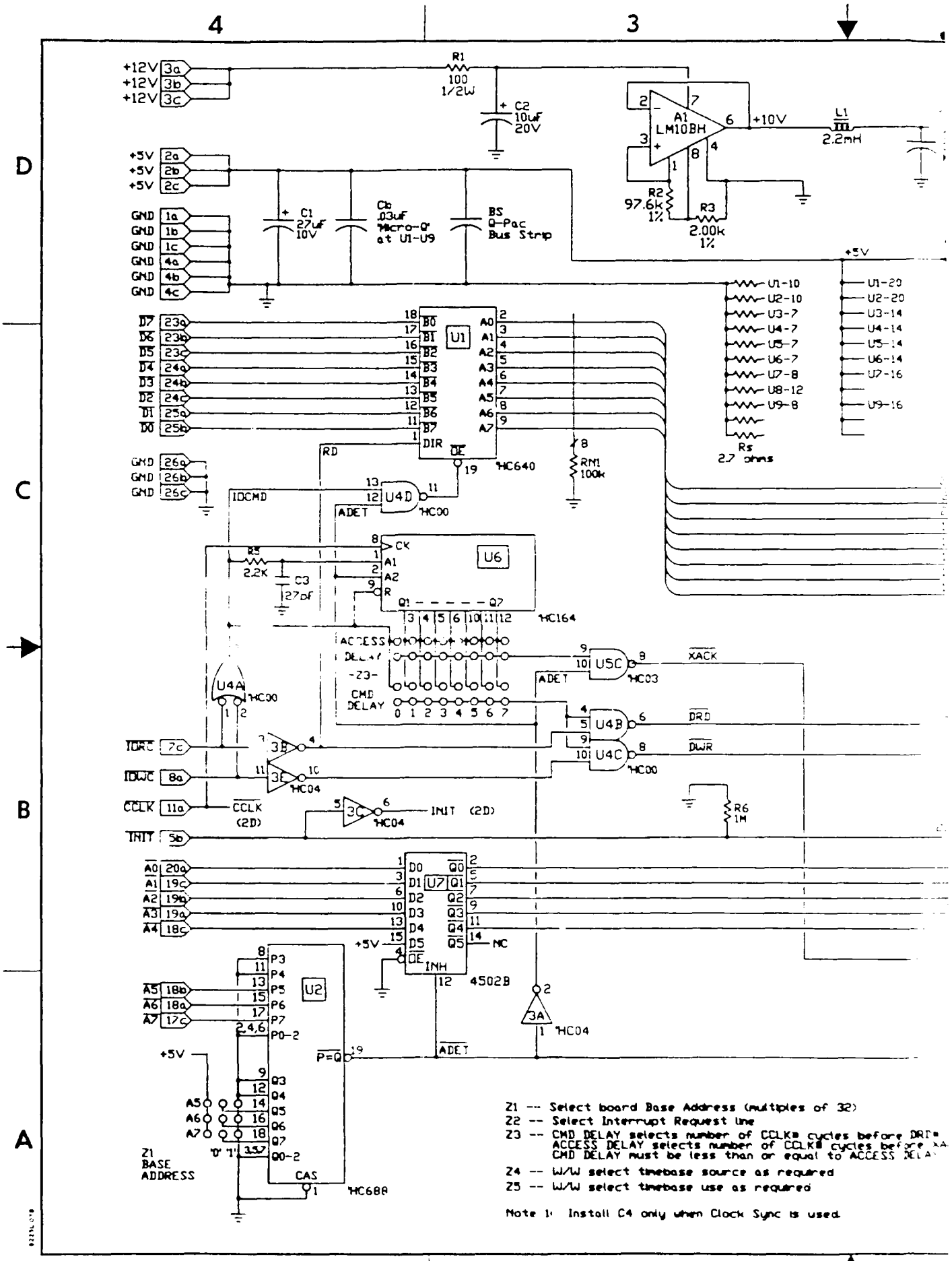
The RTC oscillator frequency is most easily set by programming the RTC for 1 Hz interrupts and adjusting C6 for precise 1 second periods at an interrupt output. If the Standby Interrupt is used, an external pullup is required on the STDBY.INTR* pin. If the INTR output is used, a simple routine that reads the RTC to clear the interrupt is required.

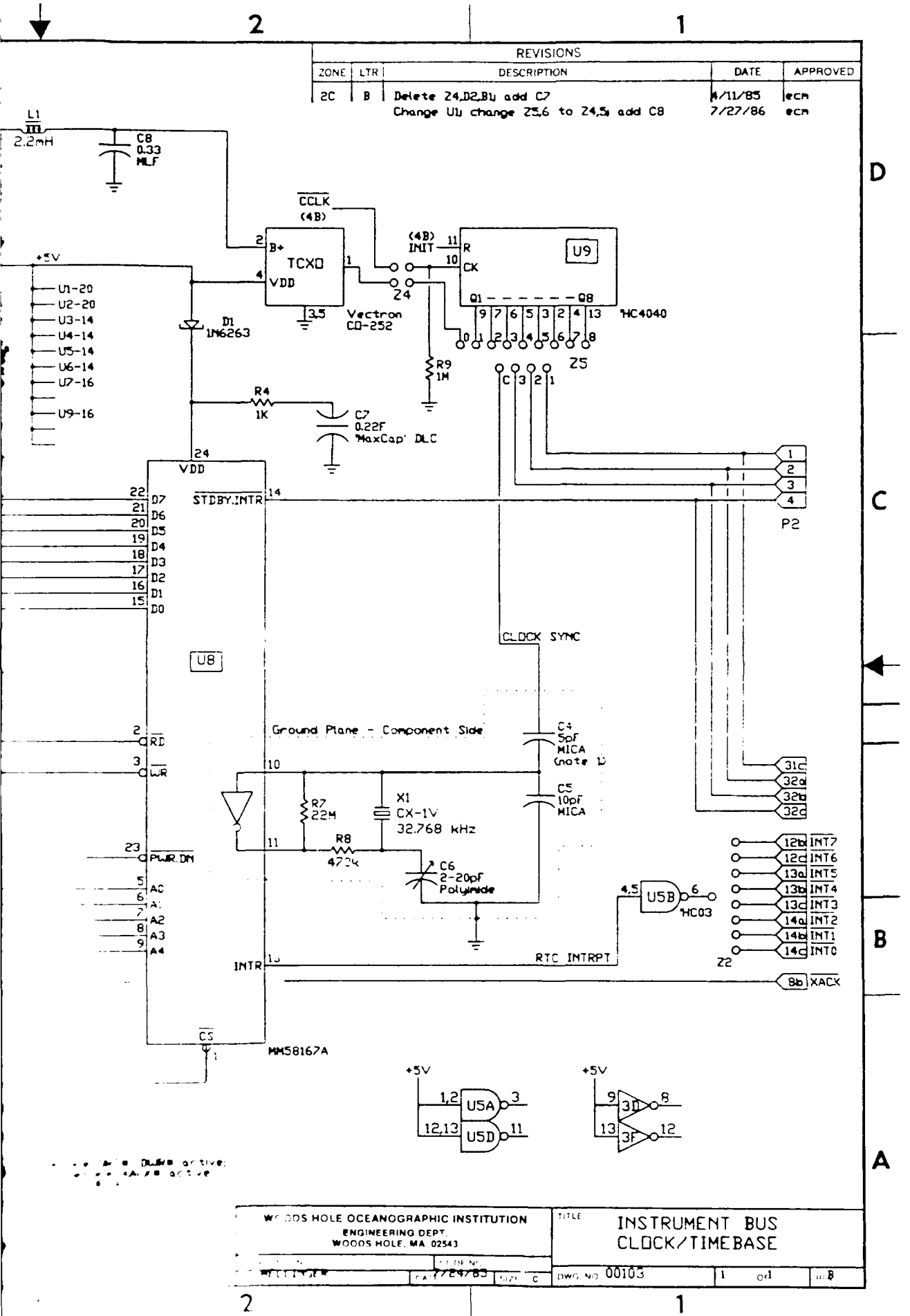
Circuit Description

Most of the IEEE-796 backplane interface, U1 - U5, is standard. U6 generates programmed wait states by clocking a 'one' level across shift register U6, in response to board Address Detect from U2 and I/O Command detect from U4A. The propagating 'one' is picked off by jumpers at selected positions on Z3 and used either to gate the I/O Command to the RTC chip, via U4B and C; or to drive the XACK handshake onto the backplane via U5C. De-assertion of the I/O Command applies Reset to U6 and terminates the I/O operation. The 50 nsec RC network between U4A and U6 prevents a race within U6 between application of the A1 Enable signal and removal of the Reset signal.

In the vicinity of the RTC chip, U7 is used to buffer and invert the chip address lines, and to disable application of chip addresses except when the Clock/Timebase board is selected. This step, and use of a 4000-series CMOS device for U7, is recommended by National Semiconductor to reduce noise coupling between RTC pins 9 and 10. Schottky diode D1 supplies operating current to the RTC with 0.3V drop, and isolates the backup supply in the event of system power loss. R4 limits charge current into double layer storage capacitor C7; the charging time constant is roughly five minutes.

A1 and associated components form a dedicated +10V linear supply for the TCXO. Other voltages are attainable by changing the ratio of R2 and R3. L1 isolates the TCXO at RF frequencies and decouples it from A1 to ensure A1 stability. The TCXO specified is a Vectron CO-252 series with logic level output, which can be ordered with any output frequency between 1 and 5 MHz..


4
3
D
C
B
A
+12V 3a
+12V 3b
+12V 3c
R1
100
1/2W
C2
10uF
20V
A1
LM10BH
+10V
L1
2.2mH
+5V 2a
+5V 2b
+5V 2c
GND 1a
GND 1b
GND 1c
GND 4a
GND 4b
GND 4c
C1
27uF
10V
Cb
.03uF
"Micro-D"
at U1-U9
BS
D-Pac
Bus Strip
R2
97.6k
1%
R3
2.00k
1%
+5V
U1-10
U2-10
U3-7
U4-7
U5-7
U6-7
U7-8
U8-12
U9-8
U1-20
U2-20
U3-14
U4-14
U5-14
U6-14
U7-16
U9-16
Rs
27 ohms
D7 23a
D6 23b
D5 23c
D4 24a
D3 24b
D2 24c
D1 25a
D0 25b
U1
B0
B1
B2
B3
B4
B5
B6
B7
DIR
OE
19
74HC640
A0
A1
A2
A3
A4
A5
A6
A7
RN1
100k
RD
GND 26a
GND 26b
GND 26c
IOCMD
U4D
74HC00
ADET
R5
2.2K
C3
27pF
U6
CK
A1
A2
R
Q1 - - - - - Q7
74HC164
ACCESS DELAY
-Z3-
CMD DELAY
0 1 2 3 4 5 6 7
U5C
XACK
U4A
74HC00
U4B
DRD
U4C
DWR
IORC 7c
IOWC 8a
74HC04
CCLK 11a
CCLK (2D)
INIT (2D)
INIT 5b
R6
1M
A0 20a
A1 19c
A2 19b
A3 19a
A4 18c
D0
D1
D2
D3
D4
D5
U7
Q0
Q1
Q2
Q3
Q4
Q5
NC
OE
INH
4502B
+5V
A5 18b
A6 18a
A7 17c
P3
P4
P5
P6
P7
P0-2
U2
P=Q
ADET
3A
74HC04
Q3
Q4
Q5
Q6
Q7
Q0-2
Z1
BASE
ADDRESS
'0' '1' 357
CAS
74HC688
Z1 -- Select board Base Address (multiples of 32)
Z2 -- Select Interrupt Request line
Z3 -- CMD DELAY selects number of CCLK8 cycles before DRD
ACCESS DELAY selects number of CCLK8 cycles before XA
CMD DELAY must be less than or equal to ACCESS DELA
Z4 -- W/W select timebase source as required
Z5 -- W/W select timebase use as required
Note 1: Install C4 only when Clock Sync is used.


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
2C | B | Delete Z4,D2,B1; add C7 | 6/11/85 | ecm
Change U1; change Z5,6 to Z4,5; add C8 | 7/27/86 | ecm
L1
2.2mH
C8
0.33
MLF
CCLK
(4B)
TCXO
B+
VDD
Vectron
CO-252
(4B)
INIT
U9
R
CK
Q1 Q8
74HC4040
Z4
Z5
D1
1N6263
+5V
U1-20
U2-20
U3-14
U4-14
U5-14
U6-14
U7-16
U9-16
R4
1K
C7
0.22F
'MaxCap' DLC
R9
1M
P2
VDD
STDBY.INTR
D7
D6
D5
D4
D3
D2
D1
D0
U8
CLOCK SYNC
Ground Plane - Component Side
C4
5pf
MICA
(note 1)
C5
10pf
MICA
X1
CX-1V
32.768 kHz
R7
22M
R8
470K
C6
2-20pf
Polyimide
RD
WR
PWR.DN
A0
A1
A2
A3
A4
INTR
RTC INTRPT
U5B
74HC03
Z2
INT7
INT6
INT5
INT4
INT3
INT2
INT1
INT0
XACK
CS
MM58167A
U5A
U5D
74HC14
WOODS HOLE OCEANOGRAPHIC INSTITUTION
ENGINEERING DEPT.
WOODS HOLE, MA 02543
TITLE
INSTRUMENT BUS
CLOCK/TIMEBASE
DWG NO 00103
SIZE C
7/24/85
1 of 1
REV B

Instrument Bus
Clock/Timebase
CE Dwg. 00103

Rev: B Date: 23 Sept 1985 By: ecm

Designation	Quan	Value	Rating	Type	Rev	Mfgr and Part Number
R1	1	100	1/2W	Carbon Comp		
R2	1	97.6k		1% RN55		
R3	1	2.00k		1% RN55		
R4	1	1k	1/4W	5% Carbon Film		
R5	1	2.2k	1/4W	5% Carbon Film		
R6,9	2	1M	1/4W	5% Carbon Film		
R7	1	22M	1/4W	5% Carbon Film		
R8	1	470k	1/4W	5% Carbon Film		
Rs	9	2.7	1/8W	Carbon Comp		Allen-Bradley 'BB'
RN1	1	100k x 9		SIP Network		Dale MSP10A01-104G
C1	1	27uF	10V	Solid Tantalum		CSR13-M39003/01-2496 (Sprague)
C2	1	10uF	20V	Solid Tantalum		CSR13-M39003/01-2526 (Sprague)
C3	1	27pF		Silver Mica		
C4	1	5 pF		Silver Mica		
C5	1	10 pF		Silver Mica		
C6	1	2.5-20pF		Polyimide Trimmer		Sprague GZL-20000 'Filmtrim'
C7	1	.22F	5V	Double Layer Cap.	B	Sohio LP055-224A 'Maxcap'
C8	1	330nF	50V	Stacked Film	C	
Cb	4	20nF	14 pin	Micro-Q		Rogers uQ-14.02
Cb	2	30nF	16 pin	Micro-Q		Rogers uQ-16.03
Cb	2	30nF	20 pin	Micro-Q		Rogers uQ-20.03
Cb	1	30nF	24 pin	Micro-Q		Rogers uQ-24.03
BS	1	.1uF		Bus Strip		Rogers QV2-9.5.1(.1)
A1	1	LM10	Voltage Ref and Op Amp			National LM10 BH
L1	1	2.2mH	30mA			Renco RL1160-2200
D1	1	1N6263		Schottky		alt: Mot. MBD-702
X1	1	32.768kHz		Tuning Fork Xtal		Statek CX-1V 'A'
TCXO	1	freq as req'd				Vectron CO-252
U1	1	74HC640	Octal Inverting Transceiver			Mot. 74HC640J (DS)
U2	1	74HC688	Octal Comparator			Mot. 74HC688J (DS)
U3	1	74HC04	Hex Inverter			Mot. 74HC04J (DS)
U4	1	74HC00	Quad NAND			Mot. 74HC00J (DS)
U5	1	74HC03	Quad NAND OD			Mot. 74HC03J (DS)
U6	1	74HC164	Shift Register			Mot. 74HC164J (DS)
U7	1	4502B	Hex Tristate Inverter			Mot. 14502B (CL)
U8	1	58167A	Clock/Calendar			National MM58167AN
U9	1	74HC4040	12 Bit Ripple Counter			Mot 74HC4040J (DS)
P1	1	DIN Connector STV-C 96-M-abc				ERNI 533-402
P2	1	AmpModU 8				AMP 87578-1
Z1-Z5	54	Shunt/Wrap Post				Samtec TSW-136-07-G-S
	8	Shunt				AMP 530153-2

4.2.9 Quad Counter/Timer

OE Dwg 00105
Rev: none Date: 3 Aug 1986 By: ecm

Description

The Quad Counter/Timer provides four Harris 82C54 Programmable Interval Timer devices, each consisting of three independent 16-bit counter/timers. Provisions are made to allow the counters to be flexibly interconnected, allowing nearly any counting or timing application to be implemented. No timing or frequency source is provided on the board, however a 16-pin AmpModU connector at the board top edge, and 6 undedicated backplane connector pins at the board bottom edge, are available for either input or output of timing signals. In addition, a small (1 sq. in.) uncommitted board area is available for implementation or installation of small local oscillator circuits.

Configuration

Required for operation: Z2
Optional: Z1,3,4-7,8,9,10

Z1: CCLK* Enable
Z3: CCLK Distribution

The IEEE-796 backplane CCLK* signal can serve as a clock or timing source to the Quad Counter/Timer board. CCLK* must be locally buffered if it is used to drive more than one or two CMOS inputs on the board. A shunt plug installed at Z1 enables CCLK* to inverter U3B, after which the buffered CCLK signal is available at Z3 for on-board distribution.

Z2: Base Address

The Clock/Timebase occupies 16 locations in the IEEE-796 I/O address space. Z2 selects the board base address in this space. All four shunt plugs must be installed for correct operation. The 16 locations have the following assignments:

Base + 0	U8 Counter 0
Base + 1	U8 Counter 1
Base + 2	U8 Counter 2
Base + 3	U8 mode control
Base + 4	U9 Counter 0
Base + 5	U9 Counter 1
Base + 6	U9 Counter 2
Base + 7	U9 mode control
Base + 8	U10 Counter 0
Base + 9	U10 Counter 1
Base + 10	U10 Counter 2
Base + 11	U10 mode control
Base + 12	U11 Counter 0
Base + 13	U11 Counter 1
Base + 14	U11 Counter 2

Base + 15 U11 mode control

Z3 **CCLK Distribution** (see Z1)

Z4-7 **Counter/Timer Interconnection**

Each 82C54 device consists of three independent 16-bit counter/timer sections, each section in turn having separate CLOCK and GATE input pins and an OUTPUT pin. For flexibility, on the Quad Counter/Timer board these inputs/outputs are not hardwired in any specific pattern, but rather are brought to wrap posts adjacent to each chip. The person configuring the system can then wire-wrap any combination of inputs or outputs that is required. Pullups are provided on all uncommitted inputs, hence only those connections required by the actual application need be made.

Z8,9 **Uncommitted Input/Output**

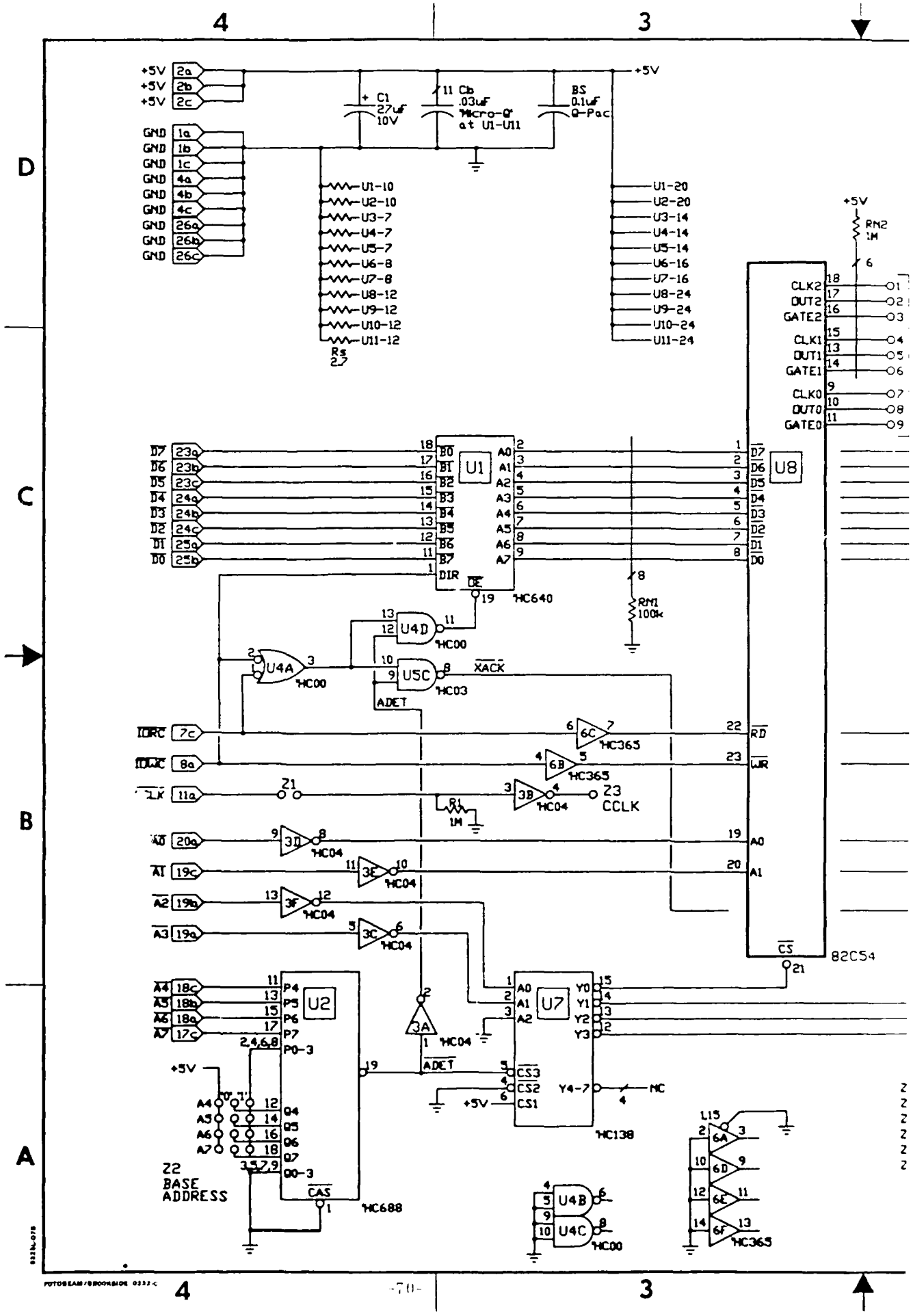
Z8 provides 16 uncommitted I/O lines via AmpModU connector P2, for signals which travel outside of the computer rack within which the board is installed. Z9 provides 6 lines via uncommitted pins on P1 (the backplane connector), for signals to or from locations within the computer rack. Z8 and Z9 are connected with wire-wrap wire to counter/timer I/O points Z4-7.

Z10 **Interrupt Select**

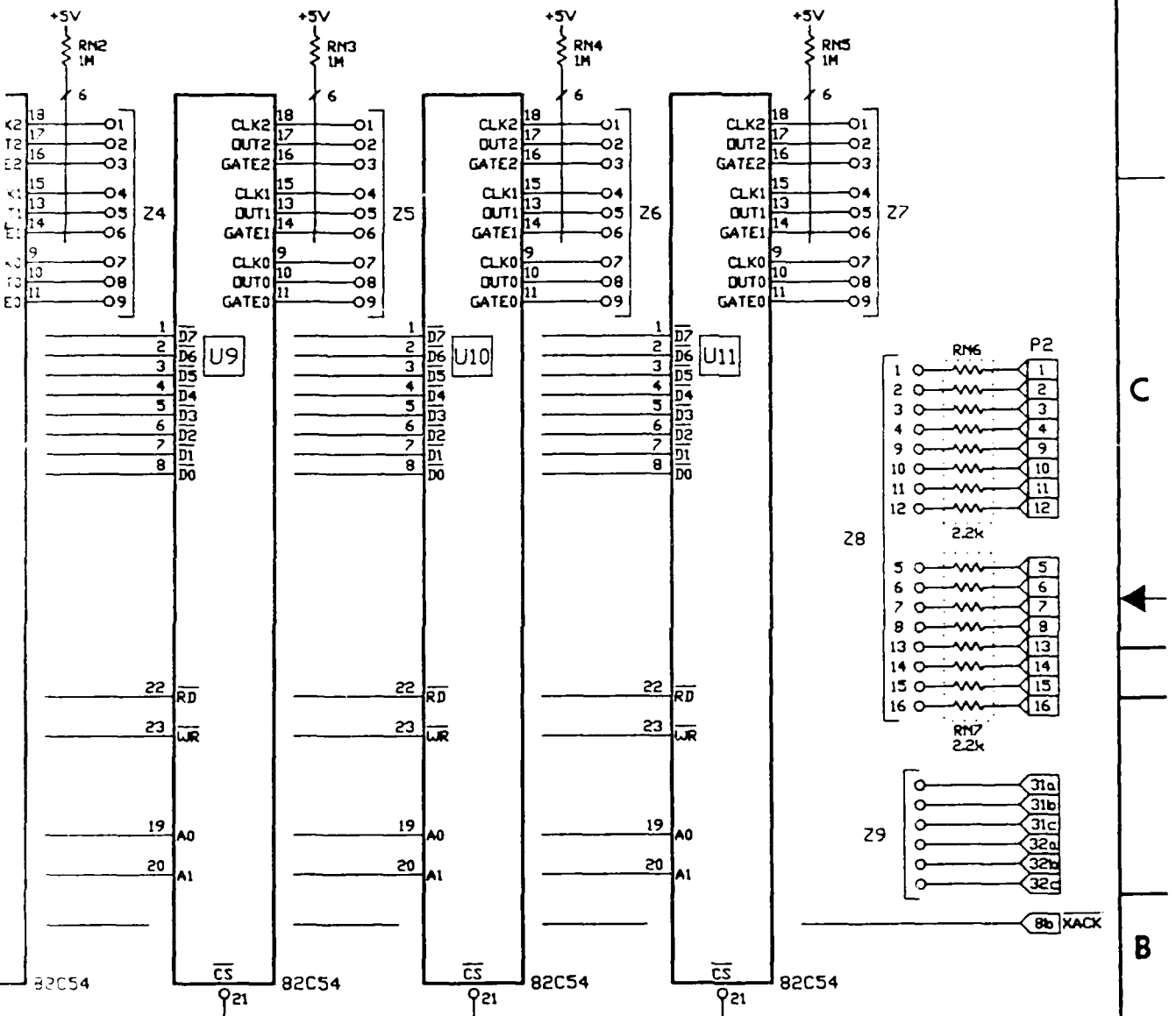
The Quad Counter/Timer board provides three uncommitted Open Drain gates (74HC03) which can be driven by any counter/timer output on the board via the IRQ A, B, C wrap posts. Z10 is then used with wire-wrap jumpers to link selected Open Drain outputs to backplane interrupt request lines INT0* - INT7*.

Circuit Description

The Quad Counter/Timer board has straightforward circuitry. The standard IEEE-796 I/O interface is formed by U1-5, with the addition of decoder U7 to handle the large number (4) of selectable I/O devices. Buffer U6 is also added to reduce loading on the backplane IORC* and IOWC* signal lines, which otherwise would have to drive all four counter/timer chips. Resistor networks RN6 and RN7 provide latch-up protection by limiting fault current to any devices connected to Z8.


4
3
D
C
B
A
+5V
GND
C1
27uF
10V
Cb
.03uF
Micro-Q
at U1-U11
BS
0.1uF
Q-Pac
U1-10
U2-10
U3-7
U4-7
U5-7
U6-8
U7-8
U8-12
U9-12
U10-12
U11-12
Rs
2.7
U1-20
U2-20
U3-14
U4-14
U5-14
U6-16
U7-16
U8-24
U9-24
U10-24
U11-24
RM2
1M
CLK2
OUT2
GATE2
CLK1
OUT1
GATE1
CLK0
OUT0
GATE0
U1
U8
DIR
OE
HC640
RM1
100k
U4D
U4A
U5C
HC00
HC03
XACK
ADET
6C
6B
HC365
RD
WR
CCLK
3D
3E
3F
3C
HC04
A0
A1
A2
A3
CS
82C54
U2
P4
P5
P6
P7
P0-3
2,4,6,8
3,5,7,9
Q4
Q5
Q6
Q7
Q0-3
CAS
HC688
22
BASE
ADDRESS
3A
U7
Y0
Y1
Y2
Y3
CS3
CS2
CS1
Y4-7
MC
HC138
U4B
U4C
L15
6A
6D
6E
6F
HC365

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		Change U1	7/27/86	ecm



Z1 -- enable CCLK to board if required
Z2 -- select board Base Address (multiples of 16)
Z3 -- W/W select CCLK as required
Z4,5,6,7 -- W/W select Timer inputs/outputs as required
Z8,9 -- W/W select board inputs/outputs as required
Z10 -- W/W select interrupt source(s) as required

WOODS HOLE OCEANOGRAPHIC INSTITUTION ENGINEERING DEPT. WOODS HOLE, MA. 02543		TITLE	INSTRUMENT BUS QUAD COUNTER/TIMER
CONTRACT NO	CODE NO		
BY MELLINGER	DATE 7/24/86 SIZE C	DWG NO 000105	1 OF 1 REV

Instrument Bus
Quad Counter/Timer
OE Dwg. 00105

Rev: none Date: 1 Aug 1985 By: ecm

Designation	Quan	Value	Rating	Type	Rev	Mfgr and Part Number
R1	1	1M	1/4W	5% Carbon Film		
Rs	11	2.7	1/8W	Carbon Comp		Allen-Bradley 'BB'
RN1	1	100k x 9		SIP Network		Dale MSP10A01-104G
RN2,3,4,5	4	1Mx6		SIP Network		Dale CSC07A01-105G
RN8	1	1M x 3		SIP Network		Dale CSC04A01-105G
RN6,7	2	2.2k x 8		DIP Network		Dale 1603-222G
C1	1	27uF	10V	Solid Tantalum		CSR13-M39003/01-2496 (Sprague)
Cb	3	20nF	14 pin	Micro-Q		Rogers uQ-14.02
Cb	2	30nF	16 pin	Micro-Q		Rogers uQ-16.03
Cb	2	30nF	20 pin	Micro-Q		Rogers uQ-20.03
Cb	4	30nF	24 pin	Micro-Q		Rogers uQ-24.03
BS	1	0.1uF		Bus Strip		Rogers QV2-9.5.1(.1)
U1	1	74HC640	Octal Inverting Transceiver			Mot. 74HC640J (DS)
U2	1	74HC688	Octal Comparator			Mot. 74HC688J (DS)
U3	1	74HC04	Hex Inverter			Mot. 74HC04J (DS)
U4	1	74HC00	Quad NAND			Mot. 74HC00J (DS)
U5	1	74HC03	Quad NAND OD			Mot. 74HC03J (DS)
U6	1	74HC365	Hex Buffer			Mot. 74HC365J (DS)
U7	1	74HC138	3-8 Decoder			Mot. 74HC138J (DS)
U8,9,10,11	4	82C54	Counter/Timer			Harris ID-82C54
P1	1	DIN Connector STV-C 96-M-abc				ERNI 533-402
P2	1	AmpModU 16				AMP 87578-5
Z1-8	76	Shunt/Wrap Post				Samtec TSW-136-07-G-S
	4	Shunt				AMP 530153-2

4.2.10 9516 A/D Control

OE Dwg 00122
Revision: none Date: 2 April 1985 By: rlk

Description

The 9516 A/D Control board, with its companion 9516 A/D Converter board, forms a two-board, 16-bit A/D converter system, with optical isolation between the two boards. The Control board resides on the IEEE-796 backplane and provides the data and control interface between the converter board and the host system via a pair of 82C55A parallel ports. The functions performed include conversion start, conversion status, and read converted data as separate 8-bit bytes. In addition, power supply control signals generated by the Control board enable the A/D board, or the entire analog front end, to be powered up or down on command.

Configuration

Required for operation: Z1
Optional: Z2

Z1: Base Address Select

The A/D Subsystem occupies 8 locations in the IEEE-796 I/O address space. Z1 selects the base address in this space. All five shunt plugs must be installed for correct operation. The 8 locations have the following assignments:

Base + 0:	Read	read A/D low byte
Base + 1:	Read	read A/D high byte
Base + 2:	Read	A/D status and control
Base + 3:	Write	U2 mode control
Base + 4:	Write	A/D start and Mux address
Base + 5:	Write	power control and spare (U3 port B)
Base + 6:	Write	not used (U3 port C)
Base + 7:	Write	U3 mode control

Z2: Interrupt Select

The A/D subsystem can be programmed to generate an interrupt when conversion is complete and data is ready. This signal is generated by U2, buffered by U7B, and appears at the input side of Z2 as an Open Drain drive signal. Shunt plugs or wire-wrap jumpers at Z2 are used to link this signal with a selected backplane interrupt signal (INT0* - INT7*).

Application Notes

The operating mode of the 82C55A parallel ports must be set by the host processor before the A/D Subsystem can be accessed. The mode must be set after every system reset (INIT* signal activation), but once set need not be changed again during normal A/D operations. To set the operating modes:

write 0BFh to the U2 control port at address Base + 3
write 08h to the U3 control port at address Base + 7

This sequence should be performed during system initialization, along with turning off the analog power supplies (see below), in order to minimize energy consumption by the A/D subsystem.

The A/D Control board generates two logic level power control signals, which appear on the uncommitted pins of the Control board backplane connector. Normally the signal designated "A/D PWR" controls the power supplies to the A/D Converter board (+5V, +/-15V), and the signal designated "Additional PWR" controls the power supplies for the sensors and signal conditioning circuits. Logic on the A/D Control board prevents Additional Power from being turned on unless the A/D Power is on also. The power control signals are accessed by a Write to U3 port B at address Base + 5, as follows:

byte	A/D PWR	Additional PWR
00h	off	off
01h	on	off
03h	on	on

The A/D converter and multiplexer are controlled by Writing to U3 port A at address Base + 4. Bits 0-5 select the input channel, with bits 0-3 allocated to the mux address and bits 4 and 5 used to select one of four multiplexers (note that only one mux, usually mux 0, is present on the A/D board). Bit 6 is reserved for future expansion and should be set to zero. Bit 7 controls the A/D converter; a transition from 0 to 1 of this bit starts the conversion sequence. The bit must be reset to 0 before it can have a transition from 0 to 1. The channel select bits (bits 0-5) must be sent or repeated each time the A/D Start bit (bit 7) is changed. Bit 7 can be reset to 0 at any time, but the channel select bits should not be changed for 40 microseconds (typical; 70 to be on the safe side) after the A/D is started, to make sure the track/hold circuit is in hold mode.

The status of the A/D converter may be determined by reading U2 port C at address Base + 2. This provides a byte with the following status bits:

Bit 7 A/D busy. This bit is 1 if the A/D is busy, 0 if it is not.
Bit 6 I/O power. This bit is 1 if the A/D power bit is on, and 0 if the power bit is off.
Bit 5 IBF-A. Input Buffer Full port A. This bit is set to 1 if the A/D has finished, and loaded its data ready to be read. Reading the low order A/D byte (Base + 0) resets this bit to 0.
Bit 4 INTE-A. Interupt Enable port A. This bit is set to 1 when the port A interrupt is enabled, and 0 when disabled.
Bit 3 INTR-A. Interrupt port A. This bit is set when Interrupt A is enabled and the A/D has finished and loaded its data ready to be read. Reading the low order A/D byte (Base + 0) clears the interrupt and sets this bit to 0. If the Interrupt is not enabled, then this bit is 0.
Bit 2 INTE-B. Interrupt Enable port B. Not used.
Bit 1 IBF-B. Input Buffer Full port B; similar to IBF-A. This bit is set to 1 if the A/D has finished, and loaded its data ready to be read. Reading the high order A/D byte (Base + 1) resets this bit to 0.

Bit 0 INTR-B. Interrupt port B. Not used.

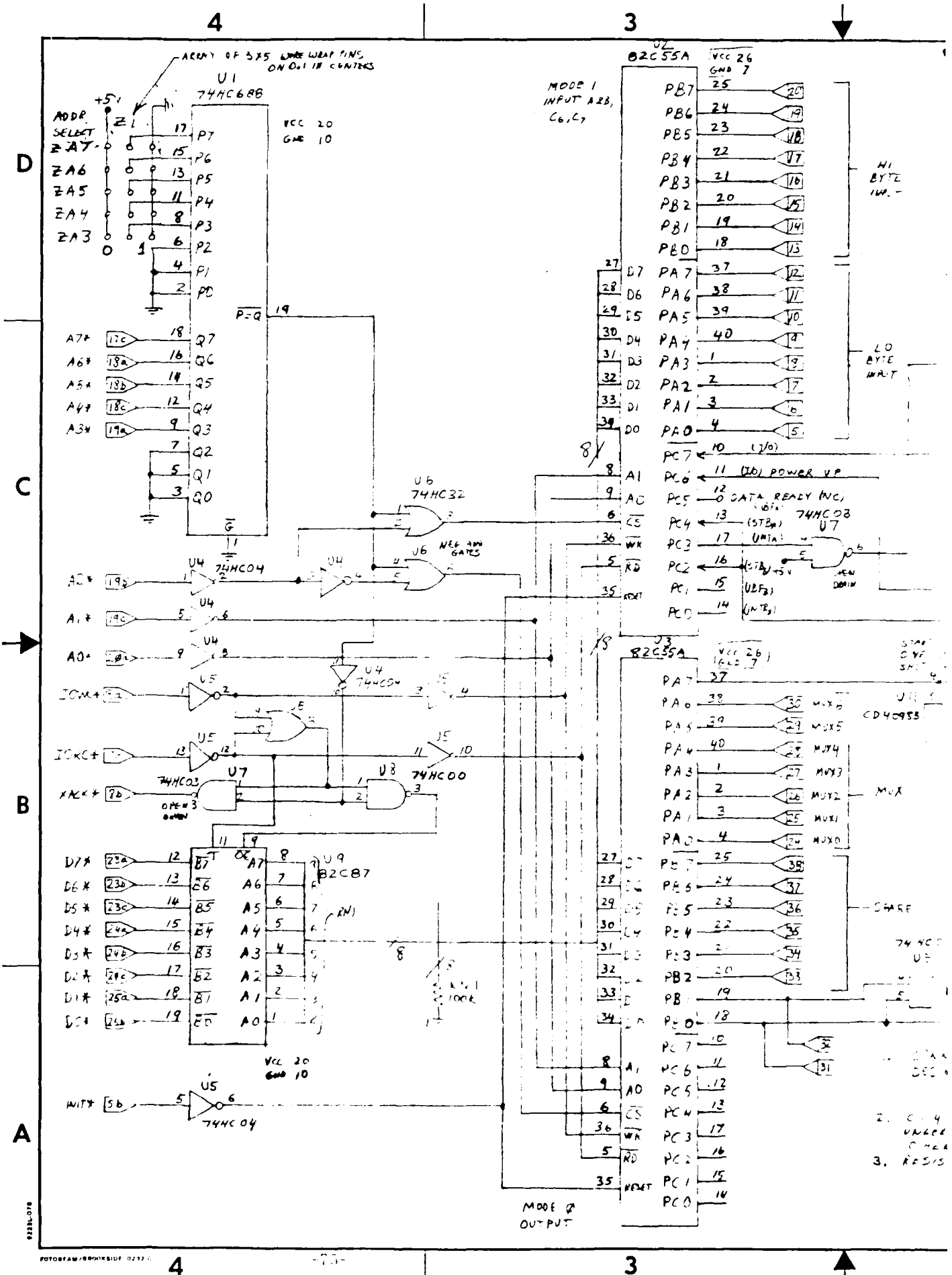
Interrupts from the A/D Subsystem are enabled or disabled by writing to the U2 control register at address Base + 3. Writing 051h sets INTE-A, which enables an interrupt from U2 on completion of the A/D conversion cycle. Writing 041h clears INTE-A, which disables the interrupt. Note that Z2 must be configured to select which backplane interrupt signal will be activated by the U2 interrupt signal INTR.

Circuit Description

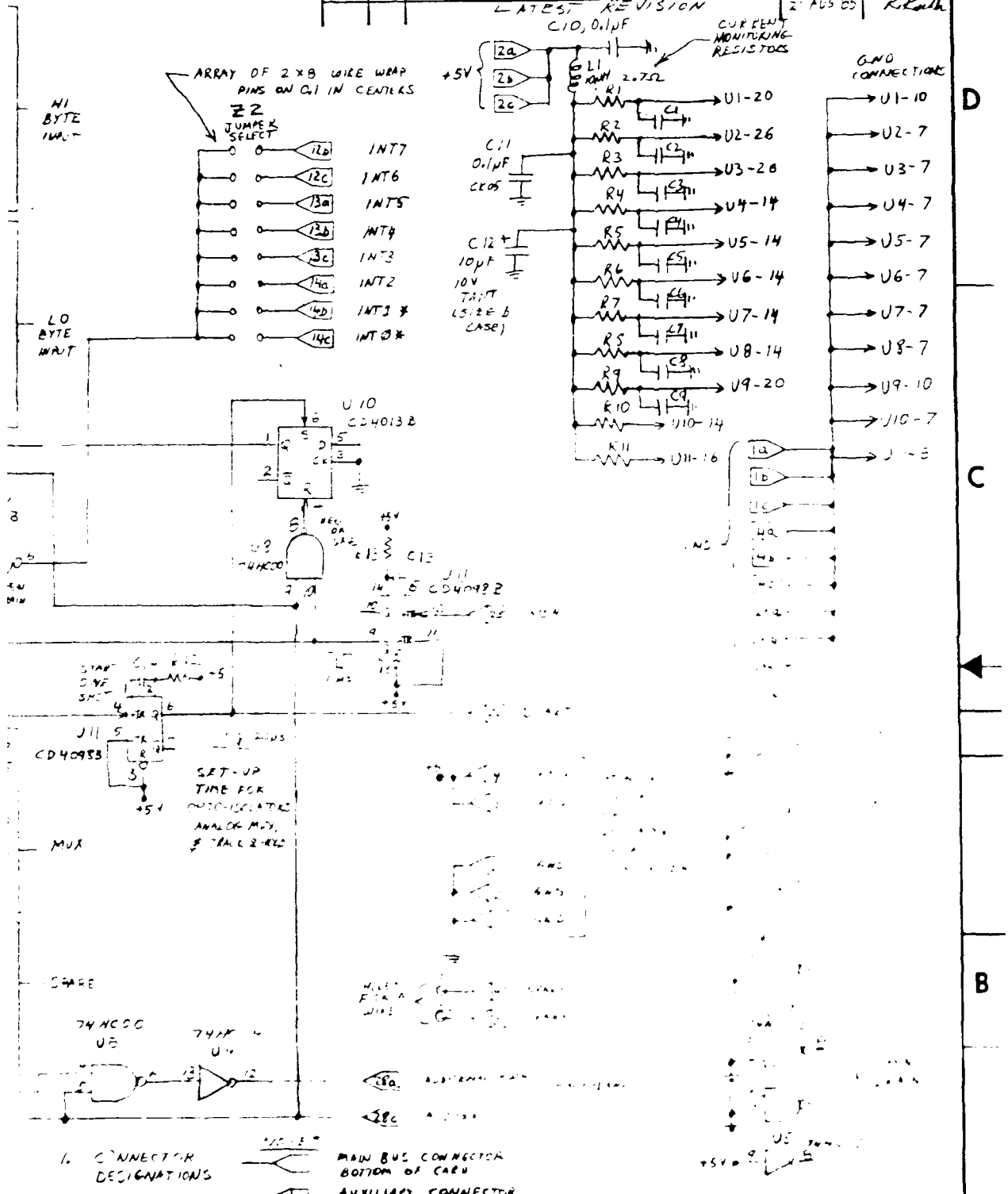
U1, U4, U5, U6, U8 and U9 on the left hand side of the 9516 A/D Control schematic form the standard IEEE-796 I/O interface with XACK* handshake. U2, an 82C55A parallel port IC, stores the A/D output which is strobed into it by the A/D converter Busy signal trailing edge (labeled FINISH on this board). U2 is programmed for Mode 1 on Ports A, B, and C. U2 port A receives the A/D low byte, and port B the high byte; thus the low byte is stored at an even I/O address and the high byte at an odd address, as required by IEEE-796. Bit 7 of U2 Port C, which indicates when the A/D converter is busy, is controlled by flip flop U10. This flip flop is set by the START pulse from U11, and is reset by the FINISH* signal from the A/D converter. Bit 6 of Port C, which indicates that the A/D power is on, is driven by the A/D PWR signal from U3, port B, bit 0.

U3, the second 82C55A parallel port, controls the starting of the A/D, the mux address, and the A/D power control signals. Ports A and B are both programmed for Mode 0 (ouput); Port C is not used. Bits 0-6 of Port A control the input channel (mux) selection. Bit 7 of port A is used to start the A/D. The rising edge of this bit triggers U11, a 20 usec one-shot. The one-shot provides setup time for the optoisolators that drive the mux address, and for the Track/Hold to acquire the new channel signal before being switched to Hold mode. U3 Port B bit 0 is available to control power to the A/D Converter board; bit 1 is available to control auxillary power. Logic in U8 and U4 prevents the auxillary power from being turned on unless the main A/D power is on. This prevents analog devices from driving signals into an unpowered mux. The rest of port B is available as spare outputs on the ribbon cable front plane.

The A/D Control board is connected to the A/D Converter board through a 40 conductor ribbon cable frontplane. This allows the A/D Converter to be located away from the very noisy computer backplane. The optocouplers on the signal lines (located on the A/D Converter board) allow the supply and ground on the A/D Control board to be separated from the supply and ground on the A/D Converter board, thereby reducing the possibiliy of noisy ground loops.


4
3
D
C
B
A
ARRAY OF 3X5 WIRE WRAP PINS ON 0.1 IN CENTERS
U1 74HC688
ADDR SELECT
ZA7
ZA6
ZA5
ZA4
ZA3
+5V
VCC 20
GND 10
P=Q
U2 82C55A
VCC 26
GND 7
MODE 1 INPUT A2B, C6,C7
HI BYTE WR
LO BYTE WRIT
U6 74HC32
U6 NEG AND GATES
U4 74HC04
U5 74HC04
U7 74HC08
U7 74HC03
U8 74HC00
OPEN DRAIN
U9 82C87
RN1 100K
U3 82C55A
CD4066B
MUX
SHARE
MODE 0 OUTPUT
INIT*
74HC04
82285-078
FOTOBEAM/BROOKSIDE
-55-

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		LATEST REVISION	2 AUG 85	R Kalb



1. CONNECTOR DESIGNATIONS
   - MAIN BUS CONNECTOR BOTTOM OF CARD
   - AUXILIARY CONNECTOR TOP OF CARD
2. C1, 4 THRU 9 ARE FLAT CAPACITORS THAT FIT UNDER THE ICS. OTHER CAPACITORS ARE CK05, UNLESS OTHERWISE SPECIFIED
3. RESISTORS ARE ¼ W CARBON COMP UNLESS OTHERWISE SPECIFIED

WOODS HOLE OCEANOGRAPHIC INSTITUTION ENGINEERING DEPT. WOODS HOLE, MA. 02543		TITLE	
CONTRACT NO	CODE NO		
BY F Kalb	DATE AUG 85	SIZE C	DWG NO	SH	REV

Instrument Bus
9516 A/D Control
OE Dwg. 00122

Rev: none Date: 2 Apr 1985 By: RLK

Designation	Quan	Value	Rating	Type	Rev	Mfgr and Part Number
R1-11	11	2.7	1/8W	Carbon Comp		Allen-Bradley 'BB'
R12	1	33k	1/4W	5% Carbon Film		
R13	1	10k	1/4W	5% Carbon Film		
RN1	1	100k x 9		SIP Network		Dale MSP10A01-104G
C10,11	2	0.1uF	50V	CK06 Ceramic		
C12	1	27uF	10V	Solid Tantalum		CSR13-M39003/01-2496 (Sprague
C13	1	100pF		Silver Mica		
C14	1	1nF	50V	CK05 Ceramic		
C2,3	0	(not used)				
C4-8	5	20nF	14 pin	Micro-Q		Rogers uQ-14.02
C1,9	2	30nF	20 pin	Micro-Q		Rogers uQ-20.03
L1	1	10uH				Renco RL-1124-.0100
U1	1	74HC688	Octal Comparator			Mot. 74HC688J (DS)
U2,3	2	82C55A	Parallel I/O Port			Harris ID-82C55A
U4,5	2	74HC04	Hex Inverter			Mot. 74HC04J (DS)
U6	1	74HC32	Quad OR			Mot. 74HC32J (DS)
U7	1	74HC03	Quad NAND OD			Mot. 74HC03J (DS)
U8	1	74HC00	Quad NAND			Mot. 74HC00J (DS)
U9	1	82C87	Octal Inverting Transceiver			Harris ID-82C87
U10	1	4013B	Dual D Flip-Flop			RCA CD4013BF (XV)
U11	1	4098B	Dual 1-Shot			RCA CD4098BF (XV)
P1	1	DIN Connector STV-C 96-M-abc				ERNI 533-402
P2	1	Amplatch 40				AMP 102326-9
W1,2	31	Shunt/Wrap Post				Samtec TSW-136-07-G-S
	6	Shunt				AMP 530153-2

4.2.11 9516 A/D Converter

OE Dwg 00120
Revision: none   Date: 4 April 1985   By: rlk

Description

The 9516 A/D Converter, with its companion 9516 A/D Control board, forms a two-board, 16-bit, optically isolated A/D converter subsystem. The Converter board resides in the analog front end rack, and is connected to the Control board in the computer rack by a private 40-conductor ribbon cable. The Converter board includes a Hybrid Systems 9516 A/D Converter (16 bits, 100 usec conversion), along with a track/hold amplifier and a 16-input analog multiplexer. Input signals are applied via the DIN backplane connector from random wiring on the analog backplane. The Converter and Control boards are optically isolated from each other on all signal lines, allowing separate grounds and power supplies to be used for the analog and computer sections of an instrument system.

Configuration

Required for operation: Z1.

Z1: **Mux Base Address**

The two most significant bits of the 6 bit multiplexer address are allocated to multi-board expansion, providing an address space of up to 64 analog input channels. Comparator U5 decodes these two bits and provides the "Mux address" function; shunt plugs or wire wrap must be installed at Z1 for proper board operation. By convention, the Mux on the Converter board is Mux [illegible] (both bits of Z1 grounded).

Application Notes

The A/D converter was selected for its 16 bit monotonicity over 0-70 degrees C; however, less expensive 15 and 14 bit monotonicity grades are available as well. The converter is subject to offset and gain drift with temperature change; since it is biased to the middle of its input range to make it bipolar, the gain drift will show up as offset drift also. For the HS9516[illegible] grade (16 bit), the bipolar zero and scale factor temperature coefficients are both +/- 10 ppm/deg C. One bit is roughly 15 ppm.

R1 and R2 are provided for offset trim adjustment of Track/Hold Amplifier U2; this adjustment can be used to zero the offset of both the T/H and the A/D converter. The adjustment is not required if DC accuracy is not required by the application. To adjust the zero, connect a [illegible]0k trimpot between U2 pins [illegible] and 4, with the wiper connected to [illegible]15V. Adjust the pot for a zero reading from the A/D converter. Measure each leg of the pot and install the closest value 1% metal film resistor in the circuit. The offset can also be zeroed in software, by periodically digitizing (and averaging, to reduce quantization noise) a Mux input which is connected to analog ground. The resulting value when subtracted from other A/D readings, will zero not only the initial

AD-A185 856 INSTRUMENT BUS: AN ELECTRONIC SYSTEM ARCHITECTURE FOR OCEANOGRAPHIC INSTRUMENTATION(U) WOODS HOLE OCEANOGRAPHIC INSTITUTION MA E C MELLINGER ET AL. 2/2

UNCLASSIFIED AUG 86 WHOI-86-30 N00014-82-C-0019 F/G 8/3 NL

END
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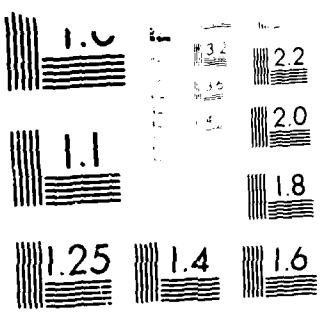

2.2
2.0
1.8
1.1
1.25
1.4
1.6

offset, but also any time or temperature dependent DC drifts in the analog chain.

A Multiplexer Expansion board to take advantage of the extra Mux select address bits has not yet been designed. Such a board would be daisy chained to the A/D Subsystem ribbon cable frontplane and would use the Channel Select signals on that bus. As an interim solution, an A/D converter board with only the multiplexer and select logic installed (no track/hold, A/D converter, or output optoisolators) can be used to perform this function.

Circuit Description

U1 is a 16-input single ended analog multiplexer with input protection. The inputs are protected even with the Mux power off; however, they will sink current in this condition and waste power from the signal source. The Mux output is connected via Track/Hold Amplifier U2 to the analog input of A/D converter U3. The converter 16-bit digital output drives optocouplers U10-U17, which are connected to the input ports on the A/D Control board via the ribbon cable frontplane. The multiplexer address lines A0-A3 are driven by the Mux Select code from the Control board, through optocouplers U6 and U7. The upper bits of the Select Code drive optocoupler U8, which is connected to magnitude comparator U5. When the Select Code equals the input from Z1, the Mux is enabled. Up to four multiplexers can be used to expand the number of analog input channels.

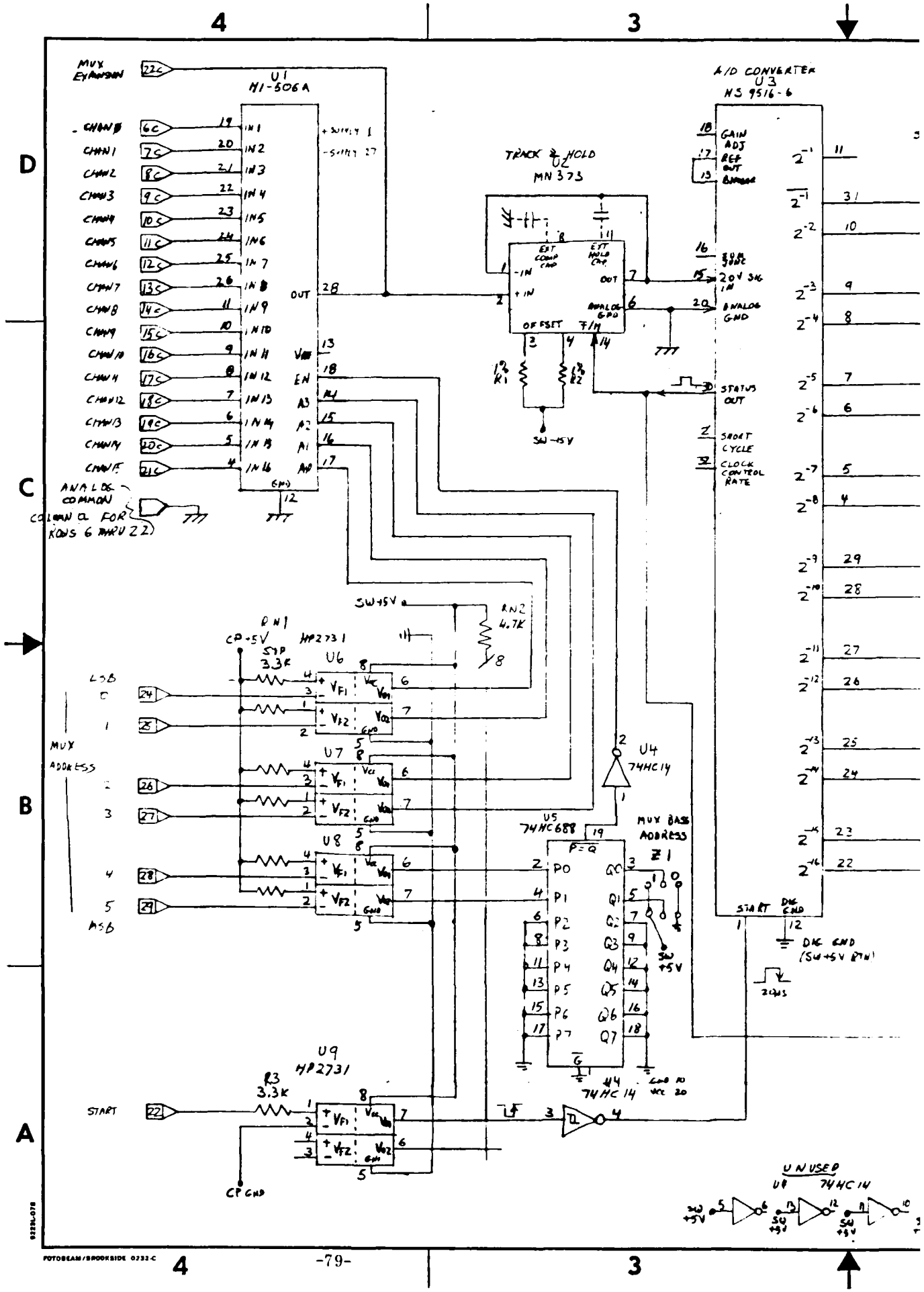
The A/D conversion cycle begins with the Start signal from the A/D Control board. This signal drives optocoupler U9, which starts the A/D converter via inverter U4B. The Busy ("Status Out") signal from the converter then switches the Track/Hold amplifier to Hold for the duration of the conversion. The Busy signal is also sent via optocoupler U18 back to the Control board; the negative transition (trailing edge) of Busy indicates that the conversion is finished.

Optical isolation allows the digital ground of the A/D converter to be disconnected from the digital ground of the computer, in order to reduce noise due to ground loops. (Note that 0.3 millivolts is one bit to the A/D, whether it appears at the signal input or on the ground pin.) The A/D converter board actually has four separate power supplies and four separate ground systems, as follows:

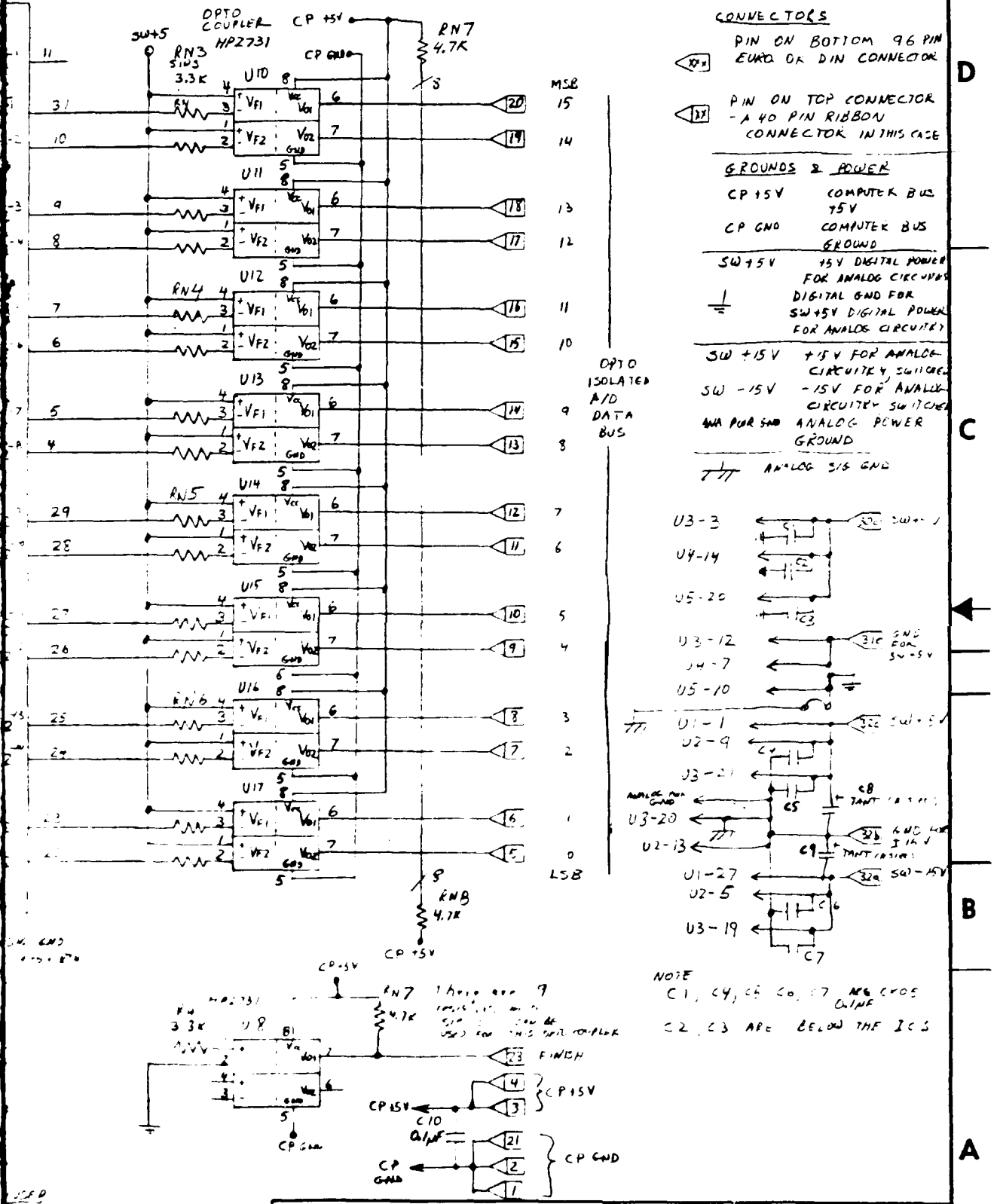
CP +5V	Computer +5V; via frontplane
CP GND	Computer Ground; via frontplane
SW +5V	+5V, switched, for digital portions of A/D; via backplane
DIG GND	SW +5V return; via backplane
SW +15V	Analog +15V, switched, for analog circuits; via backplane
SW -15V	Analog -15V, switched, for analog circuits; via backplane
ANA PWR GND	SW +/- 15V return; via backplane
ANA SIG GND	Analog signal ground; via backplane

The approximate power requirements are as follows:

SW +5V	90 mA
SW +15V	40 mA
SW -15V	29 mA


4
3
D
C
B
A
MUX EXPANSION
U1
MI-506A
CHAN 0
CHAN 1
CHAN 2
CHAN 3
CHAN 4
CHAN 5
CHAN 6
CHAN 7
CHAN 8
CHAN 9
CHAN 10
CHAN 11
CHAN 12
CHAN 13
CHAN 14
CHAN 15
OUT
ANALOG COMMON
COLUMN 0 FOR ROWS 6 THRU 22
A/D CONVERTER
U3
NS 9516-6
GAIN ADJ
REF OUT
BIPOLAR
STATUS OUT
SHORT CYCLE
CLOCK CONTROL RATE
ANALOG GND
START
DIG GND
TRACK & HOLD
U2
MN 373
OFFSET
SW -15V
RN1
HP2731
3.3K
RN2
4.7K
SW+5V
U6
U7
U8
U9
LSB
MSB
MUX ADDRESS
U5
74HC688
MUX BASE ADDRESS
U4
74HC14
UNUSED
U4 74HC14
CP GND
DIG GND (SW+5V RTN)
24µs
-79-

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		LATEST REVISION	29 JUL 85	R. Cook



WOODS HOLE OCEANOGRAPHIC INSTITUTION ENGINEERING DEPT. WOODS HOLE, MA. 02543			TITLE A/D CONVERTER	
CONTRACT NO	CODE NO			
BY [illegible]	DATE 4/AR/85	SIZE C	DWG. NO. 000120	OF / REV

Instrument Bus
9516 A/D and Mux
OE Dwg. 00120

Rev: none Date: 29 July 1985 By: RLK

Designation	Quan	Value	Rating	Type	Rev	Mfgr and Part Number
R1,2	2	10k nominal		1% RN55		Select for minimum S/H offset
R3,4	2	3.3k	1/4W	5% Carbon Film		
RN1	1	3.3k x 9		SIP Network		Dale MSP10A01-332G
RN2,7,8	3	4.7k x 9		SIP Network		Dale MSP10A01-472G
RN3,4,5,6	4	3.3k x 4	isolated	SIP Network		Dale MSP08A03-332G
C1,4-7,10	6	0.1uF		CK06 Ceramic		
C8,9	2	10uF	20V	Solid Tantalum		CSR13-M39003/01-2526 (Sprague)
C2	1	20nF		Micro-Q		Rogers uQ-14.02
C3	1	30nF		Micro-Q		Rogers uQ-20.03
U1	1	506A	16-Input Analog Multiplexer			Harris HI-1-506A-5
U2	1	373	Track/Hold Amplifier			Micro Networks MN373
U3	1	9516	16 Bit A/D			Hybrid Systems HS9516C-6
U4	1	74HC14	Hex Schmitt Inverter			Mot. 74HC14J (DS)
U5	1	74HC688	Octal Comparator			Mot. 74HC688J (DS)
U6-18	13	2731	Dual Optocoupler			HP HCPL-2731
P1	1	DIN Connector	STV-C 96-M-abc			ERNI 533-402
P2	1	Amplatch 40				AMP 102326-9

4.2.12 Terminator/Power Coupler

OE Dwg 00114
Revision: A Date: 29 July 1986 By: ecm

Description

The Terminator/Power Coupler board provides termination for three-state bus signal lines, in order to avoid floating CMOS inputs and undefined logic levels on the bus. The board also includes a power supply connector, current sense resistors, and protection circuitry ("idiot diodes") for coupling the +5V and +12V power supplies to the backplane.

Configuration

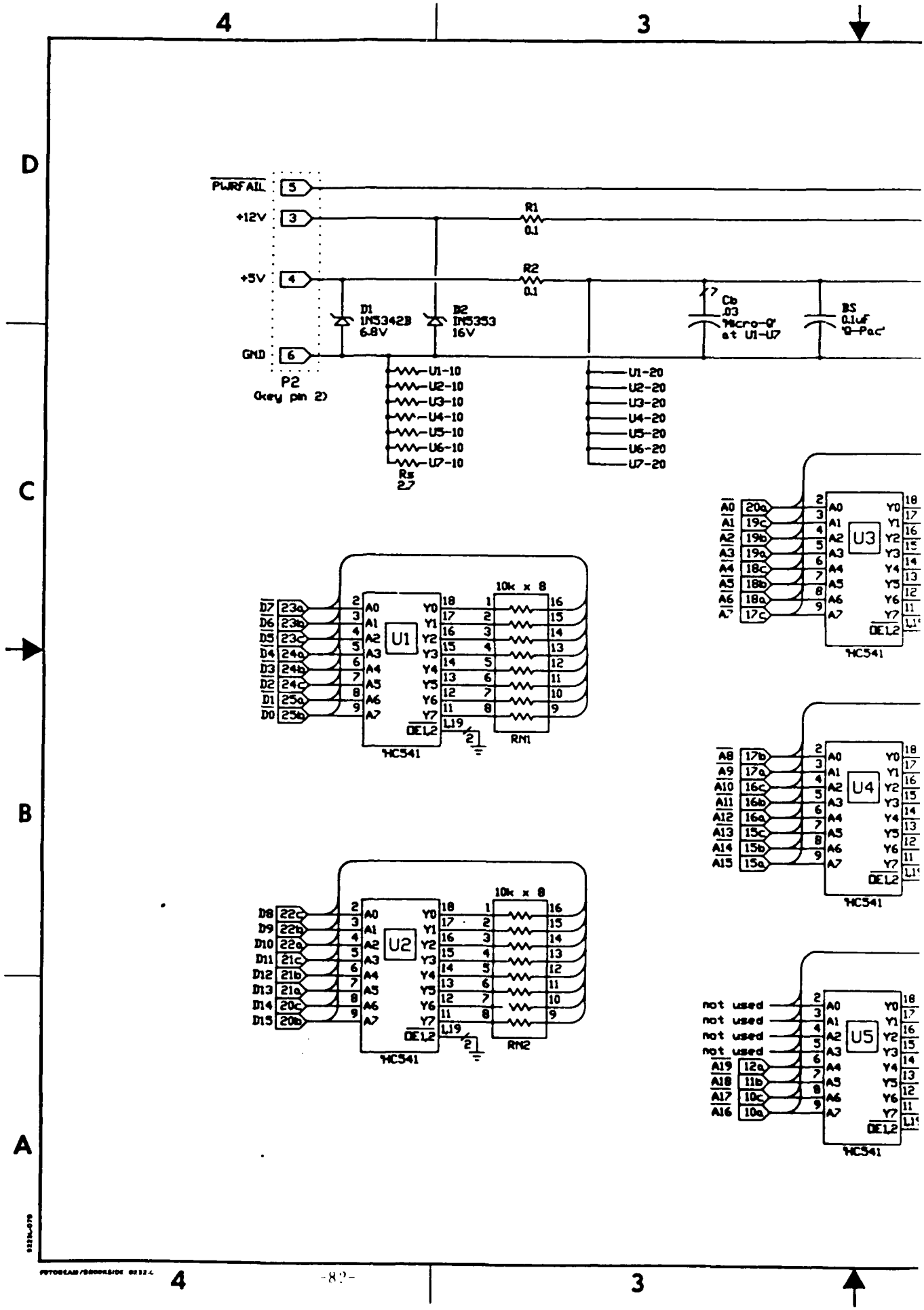
There are no wrap posts or shunt plugs to be installed on the Terminator/Power Coupler. Terminator circuits should only be installed for signal lines that will be three-stated during computer operation. Buffers U1 and U2, which terminate data bus lines D0*-D15*, should be installed for all applications. Buffers U3 through U6, which terminate the address and control bus lines, need only be installed in multimaster systems. Single-master systems normally drive the address and control busses at all times.

Application Notes

Current monitor shunts R1 and R2 enable the total supply current going into the computer backplane to measured. The value of these resistors may be changed as applications require. Idiot diodes D1 and D2 provide short-term protection from reversed or overvoltage supply inputs; they are not rated for continuous dissipation of more than a few watts and should not be counted on to do so.

Circuit Description

Each bus line terminator is simply a noninverting amplifier (buffer) with a resistor added to deliberately reduce output drive capability. The output is connected back to the input to provide positive feedback, resulting in an "overdrivable latch". This latch will maintain the last logic state applied to it, up to a specific output current (0.5 mA for the 10k resistor specified). The latch will then be overdriven and will switch to the new logic state. This active terminator circuit prevents CMOS bus lines from floating to invalid logic levels during high-impedance periods, without the static power consumption required by passive pullup terminations.


4
3
D
C
B
A
PWRFAIL 5
+12V 3
+5V 4
GND 6
P2
(key pin 2)
R1
0.1
R2
0.1
D1
1N5342B
6.8V
D2
1N5353
16V
Cb
.03
Micro-D
at U1-U7
Bs
0.1uF
D-Pac
U1-10
U2-10
U3-10
U4-10
U5-10
U6-10
U7-10
Rs
27
U1-20
U2-20
U3-20
U4-20
U5-20
U6-20
U7-20
U1
U2
U3
U4
U5
HC541
RN1
RN2
10k x 8
not used
not used
not used
not used
4
3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	Delete pullups RN8, RN9	7/29/86	ecn

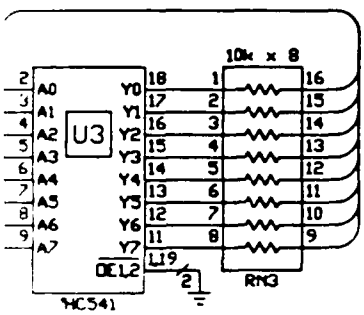
5b INIT

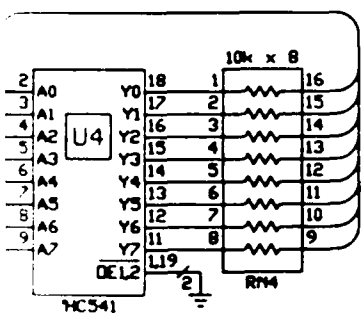
3a +12V
3b +12V
3c +12V

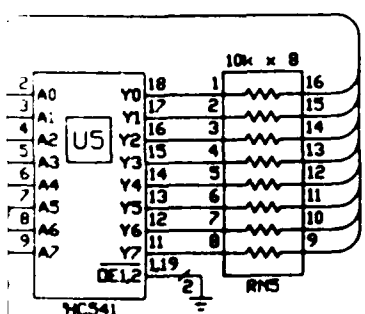
2a +5V
2b +5V
2c +5V

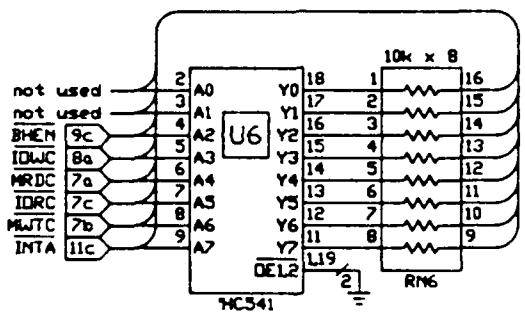
BS
0.1uf
"B-Pac"

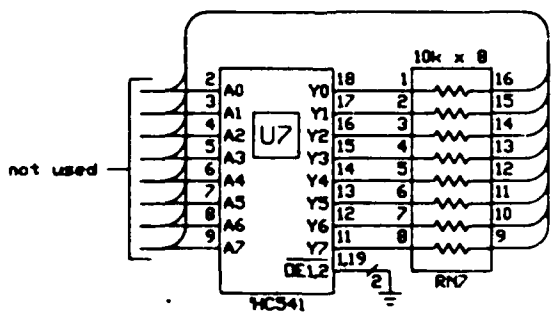
1a GND
1b GND
1c GND
4a GND
4b GND
4c GND











D C B A

WOODS HOLE OCEANOGRAPHIC INSTITUTION ENGINEERING DEPT. WOODS HOLE, MA. 02543		TITLE	INSTRUMENT BUS TERMINATOR/POWER COUPLER
CONTRACT NO	CODE NO		
BY MELLINGER	DATE 7/29/86 SIZE C	DWG NO 00114	OF REV A

2 1

Instrument Bus 1 of 1
Terminator/Power Coupler
OE Dwg. 00114

Rev: none Date: 29 July 1986 By: ecm

Designation	Quan	Value	Rating	Type	Rev	Mfgr and Part Number
R1,2	2	0.1	1/2W	1% Non-Inductive		Dale NS-1/2
Rs	7	2.7	1/8W	Carbon Comp		Allen-Bradley 'BB'
RN1-7	7	10k x 8		DIP Network		Dale MDP1603-103G
D1	1	6.8V	5W	Zener		1N5342B
D2	1	16V	5W	Zener		1N5353B
U1-7	7	74HC541	Octal Buffer			Mot. 74HC541J (DS)
P1	1	DIN Connector STV-C 96-M-abc				ERNI 533-402
P2	1	AmpModU 6 .031 x .062				AMP 87632-6

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3. STD Bus Technical Manual, Pro-Log Corporation, 2411 Garden Road, Monterey, CA 93940 (1979)

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6. R.W. Schmitt, J.M. Toole, R.L. Koehler, K.W. Doherty, and E.C. Mellinger, The Development of a new Fine- and Micro-Structure Profiler (in preparation)

7. E.C. Mellinger, High Density Static RAM for In-Situ Bulk Data Storage, Proceedings IEEE Oceans '86, Washington D.C. (1986, in press)

APPENDIX A

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Colombus, Nebraska 68601
(402) 564-3131

ERNI Components Corp.
1235 E. Davis Street
Arlington Heights, Illinois 60005
(312) 577-8620

Harris Semiconductor
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Burlington, Massachusetts 01803
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Palo Alto, California 94303-0890

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22 Linnell Circle
Billerica, Massachusetts 01821
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Waseca, Minnesota 56093
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New York, New York 10012

Micro Networks, Inc
324 Clark St.
Worcester, Massachusetts 01606
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Cambridge, Massachusetts 02140

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16. Abstract (Limit: 200 words)

A family of electronic and mechanical components has been developed to streamline the process of designing electronic systems for in-situ oceanographic instrumentation. The basis for the family is a card rack designed to fit into 6" I.D. pressure cases, and a companion CMOS computer backplane derived from the IEEE-796 (Multibus) standard. A set of computer boards based on the 80C86 processor was designed and implemented using this architecture. The board set includes the 80C86 CPU, a 64 kbyte memory module, serial and parallel I/O, timebase and counter, and a 16-bit A/D converter. A computer based on this board set consumes 375 mW at 5V while operating with a 5 MHz CPU clock, and 7.5 mW with the CPU clock in STOP mode. In addition to computers, the card rack design can also be adapted to the implementation of other electronic subsystems, including analog front end, mass storage, and power control systems. This report describes the system architecture, gives electronic and mechanical specifications for the backplane and rack, and documents each of the computer boards designed to date. (Summary portions of this report have appeared in the Proceedings of the IEEE Oceans '86 Symposium.)

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3. Computer

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